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13. SUPPLEMENTARY NOTES

14. ABSTRACT

A small, lightweight microdevice has been developed for activity-dependent stimulation (ADS) and successfully tested for functionality in both anesthetized and ambulatory rats. Further, in semi-chronic experiments in rats with traumatic brain injury (TBI) using this microdevice, an unprecedented, potent effect of ADS on motor performance has been demonstrated, as compared to control rats (injured but no microdevice) and open-loop stimulation (OLS) rats. Specifically, OLS does result in some recovery after injury, but ADS is significantly more efficacious, resulting in recovery to normal ranges of performance within 2 weeks after injury. In the final stage of this funding period, we will prepare to extend these findings to non-human primates as we finalize a) the optimal parameters for the primate TBI model and b) the design and construction of the primate microdevice.

15. SUBJECT TERMS
Anatomical rewiring; Implantable microsystem; Neuroplasticity; Rehabilitation; Traumatic brain injury

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Table of Contents

A Brain-Machine-Brain Interface for Rewiring of Cortical Circuitry after Traumatic Brain Injury

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Introduction

The goal of this project is to use an implantable brain-machine-brain interface to enhance behavioral recovery after traumatic brain injury (TBI) by reshaping long-range intracortical connectivity patterns. We hypothesize that artificial synchronous activation of distant cortical locations will encourage spontaneously sprouting axons to migrate toward and terminate in the coupled region, and that such directed sprouting can aid in functional recovery.

Body

In this section of the annual report, we describe the research accomplishments associated with each task outlined in the approved Statement of Work.

Phase IV (37-48 months), Task 1 (Electronics Testing/Microsystem Packaging)

1.1   Conduct in vivo experiments in brain-injured monkeys using a fully assembled microsystem.

As stated previously in Year 3 annual report, we have decided to use the same application-specific integrated circuit (ASIC) previously developed for rodent studies in constructing the microsystem for non-human primate (squirrel monkey) studies. This is because the capabilities of the rat ASIC (e.g., spike-stimulus time delay range, stimulus current parameters, etc) are deemed to be suitable for the initial round of experiments with non-human primates. Efforts were focused on modifying the microsystem assembly and packaging for ambulatory experiments with non-human primates, with the goal of fitting the revised microsystem inside a custom plastic chamber, as illustrated in **Fig. 1**. With internal dimensions of 18mm × 18mm, the chamber that molds to the skull curvature and spans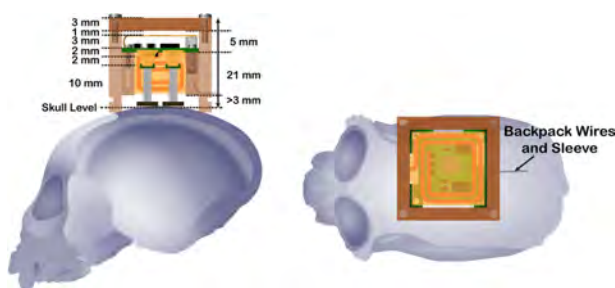 the cranial opening is attached to surround the fixed electrode connectors. This chamber serves both to protect the opening and electrodes, and to secure the microsystem. The chamber is mounted to the skull within the border of embedded skull screws and affixed with dental acrylic. The microsystem power leads are routed through a hole in the chamber and subcutaneously tunneled to the mid-scapular region of the back and into a previously installed primate jacket. These leads are then connected to a large-capacity battery pack held within the jacket. Inside the chamber, the primate microsystem connects to two multi-site, chronically implanted recording and stimulating

Figure 1. Illustration of skull-mounted plastic chamber enclosing non-human primate microsystem.

microelectrodes (NeuroNexus Technologies, Ann Arbor, MI) via two microconnectors (Omnetics Corp., Minneapolis, MN) in plug-and-play fashion, and is then screwed into place on mounting posts inside the chamber walls. After the power leads are attached to the microsystem, baseline neural data are recorded to verify functionality, and the chamber lid is screwed into place, securing all embedded microelectronic circuitry.

Our previously developed rodent microsystem featured a wired link that could be temporarily attached to the microsystem for programming and status monitoring purposes. For the non-human primate microsystem, we identified ANT radio module (ANT Wireless, Alberta, Canada) to implement such a link in wireless fashion. This would allow a home-base computer to send/receive short messages to/from the external, head-mounted

microsystem at 2.4GHz. Efforts are still focused on firmware design to develop codes for the two microcontrollers on the microsystem and external receiver board to allow bidirectional communication between the microsystem and the home-base computer via the ANT radio module.

In this section of the annual report, we describe the research accomplishments associated with tasks from previous phases as outlined in the approved Statement of Work.

Phase I (1-12 months), Task 1 (Electronics Development)

1.3   Design a neural signal processor for real-time stimulus artifact rejection using template subtraction technique with power consumption ≤5 μW.

As stated previously in Year 3 annual report, an infinite impulse response (IIR) temporal filtering technique for real-time stimulus artifact rejection (SAR) based on template subtraction was developed, optimized for hardware implementation on a field-programmable gate array (FPGA), and tested using two sets of prerecorded neural data from a rat and an *Aplysia californica* (see Appendix II). In Year 4, the SAR algorithm was integrated on an ASIC that combined spike recording, electrical microstimulation, and real-time SAR for bidirectional interfacing with 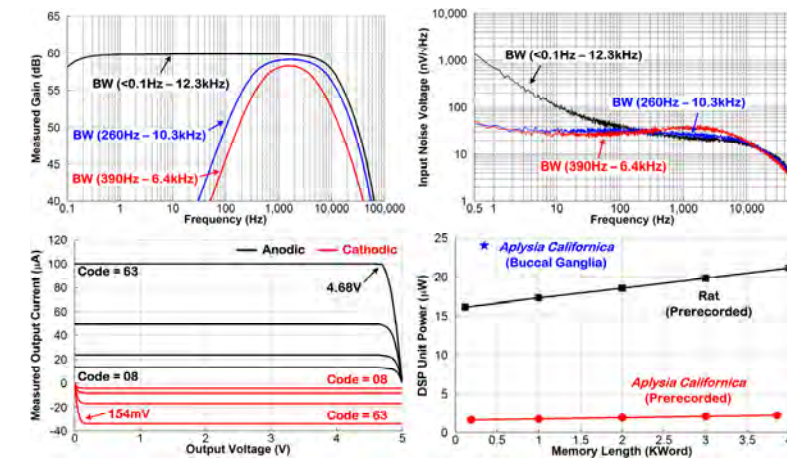the nervous system. Fabricated in AMS 0.35μm 2P/4M CMOS, the ASIC integrated a spike-recording front-end with input noise voltage of $3.42\mu V_{rms}$ (0.5Hz–50kHz), microstimulating back-end for delivering charge-balanced monophasic or asymmetric biphasic current pulses up to ~100μA with passive discharge, and μW-level digital signal processing (DSP) unit for real-time SAR based on template subtraction. The 3.1×3.1-mm^2 ASIC was characterized via benchtop tests and biological experiments in isolated buccal ganglia of an *Aplysia californica* (a marine mollusk).

Figure 2. Top – Measured gain (left) and input noise voltage (right) of the analog recording front-end. Bottom – Measured microstimulator output current *vs.* output voltage in anodic and cathodic phases (left) and DSP unit power consumption *vs.* requisite memory length for processing neural datasets from a rat and *Aplysia californica* (right).
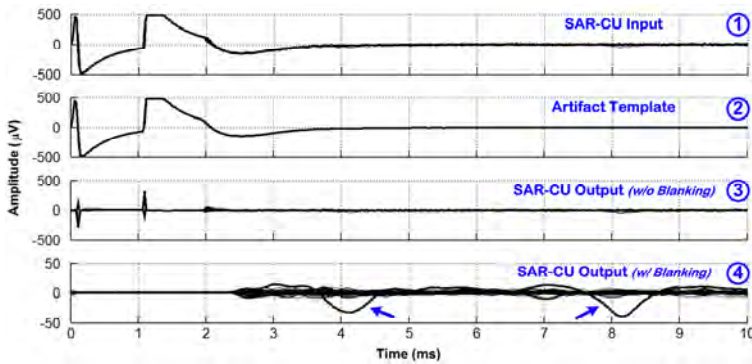

Figure 3. Measured results from neurobiological experimentation. Plot #1 shows a 10-ms window of the input data to the SAR ASIC, showing a total of 62 highpass-filtered stimulus artifacts superimposed, with some (barely visible) neural spikes riding on their tail ends. Plot #2 depicts the 62 stimulus artifact templates generated by the DSP unit and superimposed. Plot #3 shows the SAR ASIC output signal without blanking, showing significant rejection of the stimulus artifacts after template subtraction. Plot #4 shows the SAR ASIC output signal with blanking in which the neural spikes are recovered in real time after template subtraction and residual blanking (see arrows).

Fig. 2 shows measurement results from the benchtop tests. With the bandwidth of the analog recording front-end set to 390Hz–6.4kHz, the input noise voltage measured in 0.5Hz–50kHz was $3.42\mu V_{rms}$, resulting in noise efficiency factor (NEF) of 2.75. To evaluate the DSP unit power consumption, two prerecorded neural datasets from a rat (sampled at ~24.41kHz and obtained during 4-Hz cortical stimulation) and an *Aplysia californica* (sampled at 2kHz and obtained during 0.5-Hz stimulation) were used. The system clock frequency was set to ~684kHz and 56kHz for the rat and *Aplysia* datasets, respectively. **Fig. 2** shows the measured DSP unit power consumption versus requisite memory length, when processing each neural dataset for artifact removal. The measured power was in the range of 1.6–2.2μW for the *Aplysia* neural dataset and increased to 16.1–21.2μW for the rat neural dataset due to the higher system clock frequency. The SoC functionality was subsequently verified in a

neurobiological experiment with isolated buccal ganglia of an *Aplysia californica*. Custom-made hook electrodes were used for external stimulation in buccal nerve 2 (BN2) at 2Hz and recording from buccal nerve 3 (BN3). The stimulus pulsewidth was 1ms. The gain and bandwidth of the analog recording front-end were nominally set to maximum value and minimum range, respectively. The DSP unit was programmed for a low cutoff frequency of 366Hz in the digital highpass filter, *K* factor of 1/16 and blanking duration of 2.5ms synchronized with the rising edge of the *Stimulus Timing* signal. Further, the DSP unit was set to operate for 10ms in processing each artifact, which closely matched the stimulus artifact duration (obtained *a priori*) to save power consumption. **Fig. 3** depicts measured results from the neurobiological experiment, demonstrating that the SoC was fully capable of removing large stimulus artifacts in real time after template subtraction and residual blanking, and recovering the neural spikes that occurred on the tail end of the artifacts (as close as within ~4ms of stimulus onset). A statistical analysis of 60 recorded artifacts revealed an average root-mean-square (rms) value of 143µV and 6µV for the stimulus artifacts pre- and post-SAR processing, respectively, demonstrating an artifact rejection factor of ~24 by the SoC. Details of the ASIC implementation and its *in vivo* testing were published in a paper at the 2014 *IEEE Custom Integrated Circuits Conference (CICC)*, San Jose, CA (see Appendix I).

Key Research Accomplishments

- Develop a neural signal-processing algorithm for real-time stimulus artifact rejection (SAR)
- Implement the algorithm on an application-specific integrated circuit (ASIC) for real-time operation
- Demonstrate full functionality of the SAR ASIC via neurobiological experiments with an *Aplysia californica*
- Prepare and submit a paper to 2014 *IEEE Custom Integrated Circuits Conference (CICC)*, San Jose, CA. The paper was accepted and published in September 2014.

Reportable Outcomes

1- Manuscripts/Abstracts/Presentations:

- K. Limnuson, H. Lu, H. J. Chiel, and P. Mohseni, "A bidirectional neural interface SoC with an integrated spike recorder, microstimulator, and low-power processor for real-time stimulus artifact rejection," in *Proc. IEEE Custom Integr. Circ. Conf. (CICC)*, San Jose, CA, September 15-17, 2014.

- P. Mohseni, "A closed-loop brain prosthesis for functional recovery after TBI," *International Neurotechnology Consortium Workshop: Frontiers of Neurotechnology – Innovations and Translation*, *36th Annu. Int. IEEE Eng. Med. Biol. Conf. (EMBC'14)*, Chicago, IL, August 26, 2014.

- K. Limnuson, H. Lu, H. J. Chiel, and P. Mohseni, "Real-time stimulus artifact rejection via template subtraction," *IEEE Trans. Biomed. Circuits and Systems*, vol. 8, no. 3, pp. 391-400, June 2014.

- K. Limnuson, H. Lu, H. J. Chiel, and P. Mohseni, "Real-time stimulus artifact rejection via template subtraction," in *Proc. 41st Neural Interfaces Conf. (NIC'14)*, Dallas, TX, June 23-25, 2014.

- P. Mohseni, "A miniaturized brain-machine-brain interface (BMBI) for restoration of function after brain injury," *Cleveland Functional Electrical Stimulation (FES) Center Seminar Series*, Cleveland, OH, April 2, 2014.

- D. J. Guggenmos, M. Azin, S. Barbay, J. D. Mahnken, C. Dunham, P. Mohseni, and R. J. Nudo, "Restoration of function after brain damage using a neural prosthesis," *Proc. Natl. Acad. Sci. USA (PNAS)*, vol. 110, no. 52, pp. 21177-21182, December 2013.

- P. Mohseni, "A miniaturized brain-machine-brain interface (BMBI) for restoration of function after brain injury," *Institute for Neural Computation (INC) & Institute of Engineering in Medicine (IEM) Neuroengineering Seminar Series*, *University of California-San Diego*, San Diego, CA, November 4, 2013.

- D. J. Guggenmos, C. Dunham, M. Azin, S. Barbay, J. D. Mahnken, P. Mohseni, and R. J. Nudo, "Neurophysiological effects of activity-dependent stimulation following a controlled cortical impact to primary motor cortex of the rat," *Program No. 79.12, 2013 Neuroscience Meeting Planner*, San Diego, CA, Society for Neuroscience, November 2013. Online.

2- Patents and Licenses Applied for/Issued: None issued yet.

3- Degrees Obtained from Award: None yet.

4- Development of Cell Lines and Tissue/Serum Repositories: Not applicable.

5- Infomatics (Databases and Animal Models): None yet.

6- Funding Applied for: W81XWH-14-SCIRP-IIRA (Spinal Cord Injury Research Program – Investigator-Initiated Research Award) – Currently pending

7- Employment/Research Opportunities Applied for/Received: None yet.

Conclusion

Rapid progress is being made toward developing smart prosthetic platforms for altering plasticity in the injured brain, leading to future therapeutic interventions for TBI that are guided by the underlying mechanisms for long-range functional and structural plasticity in the cerebral cortex. An unprecedented, potent effect of activity-dependent stimulation (ADS) on motor performance has been demonstrated in rats with TBI. Statistical analysis of the data is complete and includes both un-implanted and open-loop stimulation control groups. Post-hoc physiological data demonstrate rapid establishment of functional connectivity between the two areas. Efforts are currently focused on developing a revised microsystem that would enable the investigation of the safety and efficacy of this approach in a non-human primate model of TBI. In parallel, we have also established the feasibility of ASIC implementation of a neural signal-processing algorithm for real-time elimination of stimulus artifacts that can potentially increase the amount of conditioning performed by the microsystem between the two cortical regions.

Appendix I   K. Limnuson, H. Lu, H. J. Chiel, and P. Mohseni, "A bidirectional neural interface SoC with an integrated spike recorder, microstimulator, and low-power processor for real-time stimulus artifact rejection," in *Proc. IEEE Custom Integr. Circ. Conf. (CICC)*, San Jose, CA, September 15-17, 2014.

A Bidirectional Neural Interface SoC with an Integrated Spike Recorder, Microstimulator, and Low-Power Processor for Real-Time Stimulus Artifact Rejection

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Abstract-**This paper presents a neural interface system-on-chip (SoC), featuring combined spike recording, electrical microstimulation and real-time stimulus artifact rejection (SAR) for bidirectional interfacing with the central nervous system. Fabricated in AMS 0.35μm 2P/4M CMOS, the SoC integrates a spike-recording front-end with input noise voltage of 3.42μV$_{rms}$ (0.5Hz–50kHz), microstimulating back-end for delivering charge-balanced monophasic or asymmetric biphasic current pulses up to ~100μA with passive discharge, and μW-level digital signal processing (DSP) unit for real-time SAR based on template subtraction. The 3.1 × 3.1-mm^2 SoC has been characterized in benchtop tests and neurobiological experiments in isolated buccal ganglia of an *Aplysia californica* (a marine sea slug). The SoC can successfully remove large stimulus artifacts from the contaminated neural data in real time and recover extracellular neural spikes that occur on the tail end of the artifacts. The root-mean-square (rms) value of the pre-processed stimulus artifact is reduced on average by a factor of ~24 post-processing.**

I. INTRODUCTION

Stimulus artifact rejection (SAR) is an integral feature of the next-generation neural interface microsystems that aim to combine electrical stimulation and neuroelectrical recording on a single chip. This is because the large stimulus artifacts can corrupt or mask the neural activity of interest, either hindering the analysis of stimulus-evoked recorded data, or limiting the efficacy of activity-dependent stimulation for closed-loop operation [1].

Blanking techniques in which the recording amplifier input is simply disconnected during stimulation have traditionally been effective in rejecting large stimulus artifacts at the expense of no viable recording during stimulation [2]. Providing a low-impedance discharge path for the stimulating electrode using active feedback circuitry [3], as well as careful design of the stimulator in terms of isolation of stimulation channels and parasitic current injection [4] can decrease the duration and amplitude of otherwise-saturating stimulus artifacts. However, these approaches cannot fully eliminate them, often leaving behind considerable residual artifacts.

On the other hand, more complex subtraction techniques have employed digital signal processing (DSP) algorithms to generate a high-fidelity template signal representative of the stimulus artifacts for subsequent subtraction from the contaminated neural data to fully remove the artifacts [5]. This is based on the premise that the overall shape, dynamic range and timing of the artifacts do not significantly vary with time.

As such, subtraction techniques rely on full-scale recording of the stationary stimulus artifacts for accurate template signal generation and are typically run offline on a home-base computer, but offer the advantage of retaining signal information during stimulation.

We have previously developed a hardware-efficient SAR algorithm based on template subtraction and successfully implemented it on an FPGA post-optimization [6]. In this paper, we present a low-power DSP architecture for integrated realization of this SAR algorithm that is incorporated into a bidirectional neural interface system-on-chip (SoC) featuring low-noise neural recording, programmable neurostimulation and real-time stimulus artifact removal.

II. SYSTEM ARCHITECTURE

Fig. 1 shows the system architecture of the proof-of-concept, bidirectional neural interface SoC that comprises a spike-recording front-end, a programmable microstimulator and an embedded DSP unit. The system is designed to operate from 1.5V, except for the stimulating electrode driver stage in which 5V is used for enhanced voltage compliance.

The recording front-end performs ac amplification, dc baseline stabilization, highpass filtering and 10b digitization of the neural data with digitally programmable gain and bandwidth. The microstimulator delivers trains of charge-balanced monophasic or asymmetric biphasic current pulses followed by passive discharge, with digitally programmable current pulse amplitude and externally controllable current pulse duration, frequency and number within a stimulus train.

The DSP unit performs additional highpass filtering digitally to remove any residual dc offset or low-frequency noise, and performs real-time stimulus artifact removal based on template subtraction. To generate a template signal representative of the stimulus artifacts, infinite impulse response (IIR) temporal filtering is employed in the form of an exponentially weighted moving average (EWMA) of several properly shifted versions of the input neural data containing the stimulus artifacts [6]. This can be represented by:

$$y_n = (1 - K).y_{n-1} + K.x_n, \qquad (1)$$

where y_n is the new artifact template signal, y_{n-1} is the previous template signal and x_n is the input neural data. Factor $K < 1$ affects the IIR system response time and accuracy.
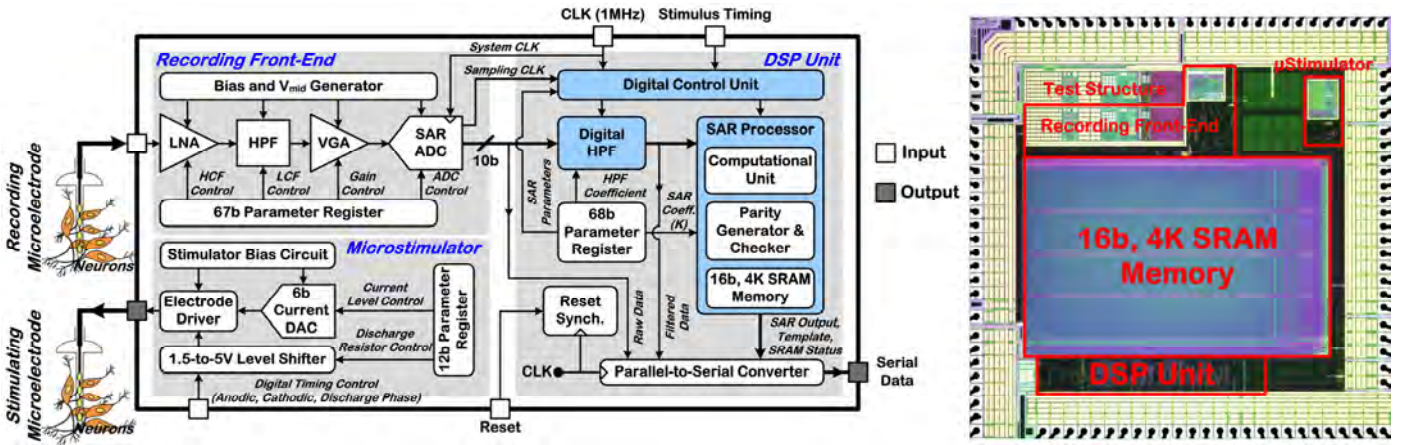
Fig. 1. System architecture and die micrograph of the bidirectional neural interface SoC fabricated in AMS 0.35µm 2P/4M CMOS.

Hence, the template signal is retained in a memory, and a new template signal is generated from the previous template signal and the input neural data according to (1), which is then subtracted from the input neural data.

III. INTEGRATED CIRCUIT ARCHITECTURE

A. Recording Front-End

Fig. 2 depicts the circuit schematic of the spike-recording front-end, comprising an LNA with adjustable high cutoff frequency (HCF), highpass filter (HPF) with adjustable low cutoff frequency (LCF), VGA with adjustable offset and 10b SAR ADC. It features an overall bandpass frequency response with eight different gain values in 49–65.6dB at 1kHz, with the LNA providing fixed 32dB of ac gain via capacitive feedback and dc baseline stabilization via a MOS-bipolar pseudo resistor in parallel with the feedback capacitor. With the ac gain nominally set to 60dB, the bandwidth (BW) can be programmed from <0.1Hz–12.3kHz to 390Hz–6.4kHz by digitally tuning the HPF and LNA bias currents. The SAR ADC is nominally clocked at 1MHz, with each ADC conversion cycle taking 28 clock cycles to relax current drive requirements of the preceding VGA for low-power operation, thus providing a nominal sampling frequency of 35.7kSa/s.

B. Microstimulator

The electrical microstimulator comprises a 6b current-based DAC, electrode driver, 12b parameter register, signal level shifter and bias circuitry. The electrode driver operates from 5V and integrates a pair of pMOS (anodic) and nMOS (cathodic) current sources with thick-oxide transistors and boosted output impedance (>100MΩ) via negative feedback for constant-current stimulation [1]. The DAC operates from 1.5V and outputs a programmable current in 0–2.2µA with 6b resolution, which is then amplified to generate a maximum current of ~100µA for the anodic phase. The cathodic-phase current is set to be 1/3 of that in the anodic phase via proper transistor sizing ratios to generate an asymmetric biphasic current pulse for optimal use of the available voltage headroom (5V).
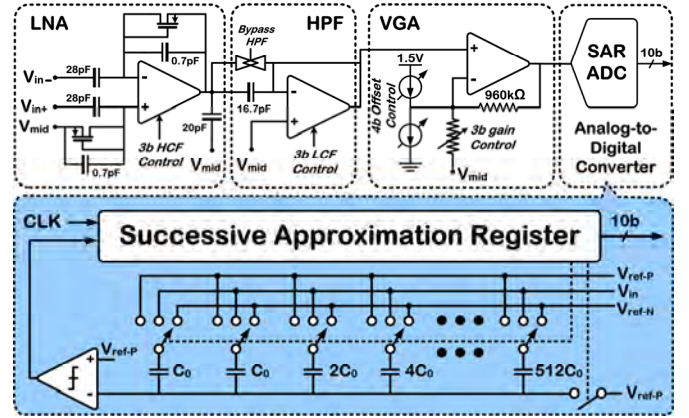

Fig. 2. Circuit schematic of the spike-recording front-end.

C. DSP Unit

The major building blocks of the DSP unit include a digital HPF, digital control unit and a SAR processor, which in turn comprises a computational unit, SRAM (16b, 4K) and parity generator/checker to identify potential memory errors. A 68b parameter register is used to store user-set parameters such as the bandwidth setting of the digital HPF and SAR coefficient K, as well as memory-initialization, memory-length and output-blanking settings. The requisite memory length (i.e., # of 16b samples) depends on the sampling frequency and time duration over which the SAR algorithm operates, which should be at least equal to the stimulus artifact duration for proper operation. With a nominal sampling frequency of 35.7kSa/s in the recording front-end, the DSP unit can process stimulus artifacts as long as ~115ms in duration.

Fig. 3 depicts the structure of the digital HPF and SAR processor in the DSP unit. The digitized neural sample (10b) from the ADC is first highpass filtered using a 1st-order filter with direct form II architecture and adjustable LCF. Factor K_1 can be set as 1/16 or 1/8, resulting in a LCF of 366 or 756Hz, respectively, with a 1-MHz clock. An overflow/underflow detector is used at the HPF output to limit its dynamic range to 10b before feeding it to the SAR processor.
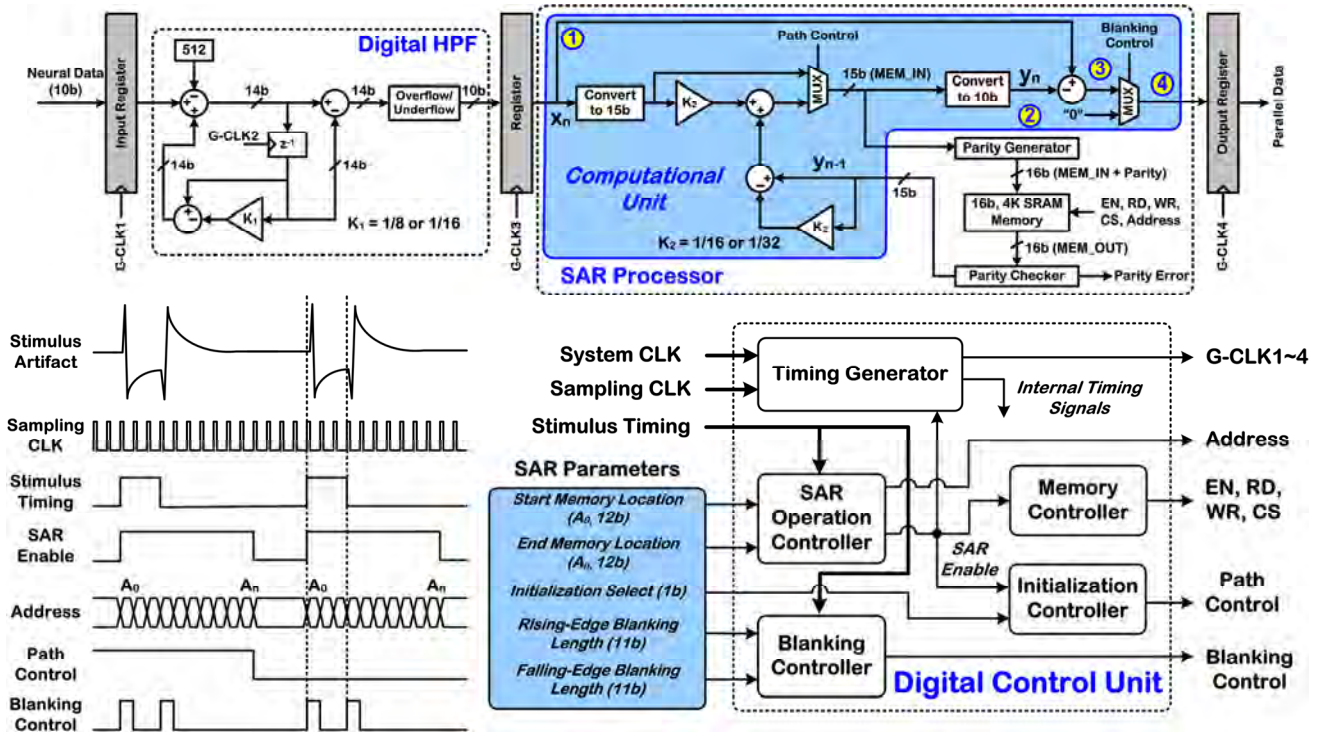
Fig. 3. Architecture of the digital HPF, SAR processor and digital controller of the DSP unit along with illustration of its timing operation.

The SAR processor only operates for the duration of each stimulus artifact and uses fixed-point computation for simplicity, with 15b representation at its internal nodes to mitigate quantization noise effects on template signal accuracy [6]. The digitized/filtered sample at the HPF output (10b) is first converted to 15b and then multiplied by factor K_2 (same as K in (1), 1/16 or 1/32 in this work) stored in the 68b parameter register. Next, the memory data containing the previous template signal are read, multiplied by $(1-K_2)$ and added to $(K_2 . x_n)$ to obtain the new template signal (15b), which is written back into the 16b memory for the next cycle after an even-parity bit addition. The new template signal is also converted back to 10b and subsequently subtracted from the 10b digitized/filtered input sample to produce the SAR output signal. Outside the duration of the artifact, the SAR processor is disabled, and the sample at the HPF output is directly routed to the output register.

Using the *Stimulus Timing* signal and *Path Control* from the digital control unit, the computational unit of the SAR processor (SAR-CU) initializes the memory with the very first recorded stimulus artifact, which is shown to significantly decrease the response time of the IIR-SAR algorithm in generating an accurate template signal, especially when stimulus artifacts are highly reproducible in consecutive stimulation cycles [6]. Further, using the *Stimulus Timing* signal and *Blanking Control* from the digital control unit, the SAR-CU can remove any residual artifacts in the output after template subtraction, especially at the rising and falling edges of the artifact where it rapidly changes with time. With two 11b parameters, the user can independently set the blanking duration from 0 (i.e., no blanking) to 2,047 data points, synchronized with the rising and falling edges of the *Stimulus Timing* signal.

The three registers in Fig. 3 are used for holding the data for processing in each stage with proper timing control. As compared to the strategy of sharing the same clock signal globally and using a local enable signal for synchronizing these registers [6], clock gating is used instead for reduced power consumption.

Fig. 3 also depicts the structure of the digital controller in the DSP unit along with its timing operation for two consecutive stimulus artifacts assumed to be the very first and second artifacts (see the *Path Control* signal.) The digital control unit comprises a timing generator and several controllers to manage the SAR processor operation, memory operation and its initialization, and output blanking.

The timing generator creates all internal timing signals for the digital control unit, as well as the gated clocks for the digital HPF and the three registers. The SAR operation controller detects the rising edge of the *Stimulus Timing* signal and subsequently generates the internal *SAR Enable* signal. The SAR processor only operates when *SAR Enable* is high, which is programmable via the user-set memory-length setting and should be ideally equal to the stimulus artifact duration (and not much longer) to save processing power. The SAR operation controller also generates the *Address* signal to access the memory between the start (A_0) and end (A_n) locations. As mentioned previously, the SAR processor is disabled when *SAR Enable* is low (i.e., outside the stimulus artifact duration).

IV. MEASUREMENT RESULTS

A prototype chip was fabricated in AMS 0.35µm 2P/4M CMOS, measuring ~3.1 × 3.1mm^2 including the bonding pads (see Fig. 1.) The chip was first tested during benchtop measurements as shown in Fig. 4. With the BW of the analog recording front-end set to 390Hz–6.4kHz, the input noise voltage measured in 0.5Hz–50kHz was 3.42µV$_{rms}$, resulting in noise efficiency factor (NEF) of 2.75 for the LNA. To evaluate the DSP unit power consumption, two *prerecorded* neural datasets from a rat (sampled at ~24.41kHz and obtained during 4-Hz cortical stimulation) and an *Aplysia californica* (sampled at 2kHz and obtained during 0.5-Hz stimulation) were used. The system clock frequency was set to ~684 and 56kHz for the rat and *Aplysia* datasets, respectively (i.e., 28× their sampling frequency). Fig. 4 shows the measured DSP unit power consumption versus requisite memory length, when processing each neural dataset for artifact removal. The measured power was in the range of 1.6–2.2µW for the *Aplysia* neural dataset and increased to 16.1–21.2µW for the rat neural dataset due to the higher system clock frequency. Within each dataset, the measured power also increased with the time duration over which the *SAR Enable* signal was high.

The SoC functionality was subsequently verified in a neurobiological experiment with isolated buccal ganglia of an *Aplysia californica* (a marine sea slug). Custom-made hook electrodes were used for external stimulation in buccal nerve 2 (BN2) at 2Hz and recording from buccal nerve 3 (BN3). The stimulus pulsewidth was 1ms. The gain and BW of the analog recording front-end were nominally set to maximum value and minimum range, respectively. The DSP unit was programmed for an LCF of 366Hz in the digital HPF, *K* factor of 1/16 and blanking duration of 2.5ms synchronized with the rising edge of the *Stimulus Timing* signal. Further, the DSP unit was set to operate for 10ms in processing each artifact, which closely matched the stimulus artifact duration (obtained *a priori*) to save power consumption. Fig. 5 depicts measured results from the neurobiological experiment, demonstrating that the SoC was fully capable of removing large stimulus artifacts in real time after template subtraction and residual blanking, and recovering the neural spikes that occurred on the tail end of the artifacts (as close as within ~4ms of stimulus onset). A statistical analysis of 60 recorded artifacts revealed an average root-mean-square (rms) value of 143µV and 6µV for the stimulus artifacts pre- and post-SAR processing, respectively, demonstrating an artifact rejection factor of ~24 by the SoC.

V. CONCLUSION

This paper reported on a bidirectional neural interface SoC for combined spike recording, electrical microstimulation and real-time stimulus artifact rejection (i.e., as the recording is taking place). The SoC integrated a low-power DSP unit that generated a high-fidelity template signal representative of the stimulus artifacts via temporal filtering and then subtracted it from the contaminated neural data to remove the artifacts.
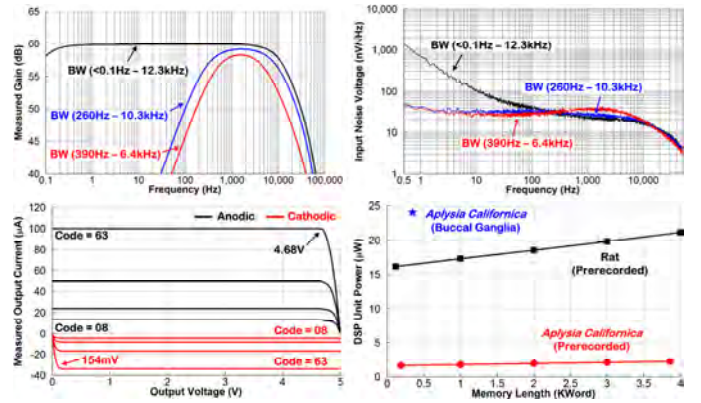

Fig. 4. Top – Measured gain (left) and input noise voltage (right) of the analog recording front-end. Bottom – Measured microstimulator output current *vs.* output voltage in anodic and cathodic phases (left) and DSP unit power consumption *vs.* requisite memory length for processing neural datasets from a rat and *Aplysia californica* (right).
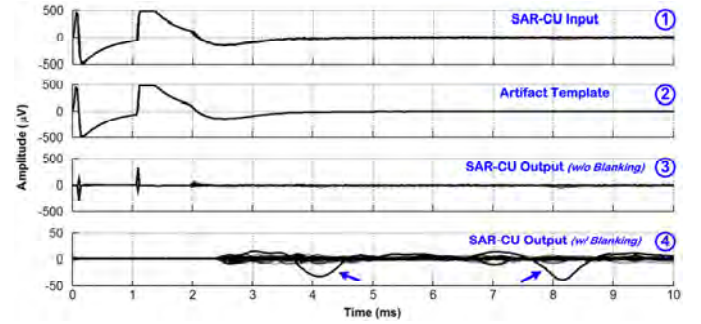

Fig. 5. Measured results from neurobiological experimentation. Plot numbers correspond to the node numbers in the SAR-CU of Fig. 3. Plot #1 shows a 10-ms window of the input data to the SAR-CU, showing a total of 62 highpass-filtered stimulus artifacts superimposed, with some (barely visible) neural spikes riding on their tail ends. Plot #2 depicts the 62 stimulus artifact templates generated by the DSP unit and superimposed. Plot #3 shows the SAR-CU output signal without blanking, showing significant rejection of the stimulus artifacts after template subtraction. Plot #4 shows the SAR-CU output signal with blanking in which the neural spikes are recovered in real time after template subtraction and residual blanking (see arrows).

The SoC functionality was demonstrated in biological tests with isolated buccal ganglia of an *Aplysia californica*, with a power consumption of ~27 and 24µW for the spike-recording front-end and the DSP unit, respectively, from 1.5V.

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Real-Time Stimulus Artifact Rejection Via Template Subtraction

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Abstract—This paper presents an infinite impulse response (IIR) temporal filtering technique for real-time stimulus artifact rejection (SAR) based on template subtraction. A system architecture for the IIR SAR algorithm is developed, and the operation of the algorithm with fixed-point computation is analyzed to obtain the number of bits for the internal nodes of the system, considering dynamic range and fraction length requirements for optimum performance. Further, memory initialization with the first recorded stimulus artifact is proposed and shown to significantly decrease the IIR system response time, especially when artifacts are highly reproducible in consecutive stimulation cycles. The proposed system architecture is hardware-implemented on a field-programmable gate array (FPGA) and tested using two sets of prerecorded neural data from a rat and an *Aplysia californica* (a marine sea slug) obtained from two different laboratories. The measured results from the FPGA verify that the system can indeed remove the stimulus artifacts from the contaminated neural data in real time and recover the neural action potentials that occur on the tail end of the artifact (as close as within 0.5 ms after the artifact spike). The root-mean-square (rms) value of the pre-processed stimulus artifact is reduced on average by a factor of 17 (*Aplysia californica*) and 5.3 (rat) post-processing.

Index Terms—Closed-loop neuroprostheses, field-programmable gate array (FPGA), neural recording, neurostimulation, stimulus artifact rejection, template subtraction.

I. INTRODUCTION

STIMULUS ARTIFACT REJECTION (SAR) is important in biopotential recording, whenever stimulation is performed in the same medium in which the recording electrodes are also placed [1]. This is because the large stimulus artifacts can corrupt or mask the neural activity of interest, either hindering the analysis of stimulus-evoked recorded data [1],

or limiting the efficacy of activity-dependent stimulation for closed-loop operation [2], [3]. Many SAR techniques have been developed in the past that use the same fundamental principles for rejection, and the choice of a particular method is typically dependent on the type of biopotential that is being recorded and the conditions under which the recording is taking place [4]–[7].

The two primary classes of SAR techniques are the so-called *blanking* and *subtraction* techniques. There are also some other techniques that do not readily fit into one of these two categories [8], [9]. Blanking techniques essentially disconnect the input of the recording amplifier during stimulation. Stimulation-synchronized blanking can be achieved by several methods, including grounding the amplifier input [10], [11], connecting the amplifier input to its output or to that of a sample-and-hold circuit [12], [13], digitally replacing the contaminated signal during the artifact interval with an estimate of the uncontaminated signal [14], and using high-speed auto-zeroing to maintain the amplifier output constant during stimulation [15]. In general, blanking techniques are relatively simple, effective for rejecting large stimulus artifacts, practical for preventing amplifier saturation, and inherently amenable to hardware implementation for real-time SAR. The major drawback is that recording is not viable during stimulation.

Subtraction techniques basically subtract a template signal representative of the stimulus artifacts from the contaminated neural data to remove the artifacts. These techniques do not prevent amplifier saturation on their own and often necessitate running a digital signal processing (DSP) algorithm, rendering them much more complex than the blanking techniques. The major advantage is that these techniques make it possible to retain signal information during stimulation.

Generating an accurate template signal has been the main focus of research in subtraction-based SAR techniques and can be achieved by several methods, including artifact modeling based on locally fitted cubic polynomials [5], capturing the artifact from subthreshold stimulation or from a second recording site remote from the stimulation site [1], and temporal averaging of the contaminated data for multiple consecutive stimulation cycles [16], [17], with the underlying assumption that the overall shape, dynamic range, and timing (e.g., latency with respect to the stimulus timing signal) of the stimulus artifacts do not significantly vary with time.

Subtraction techniques have the potential to fully eliminate the artifacts from the contaminated data record, but have to rely on the generation of an accurate template signal for subtraction, which in turn necessitates an adjustment in the recording amplifier gain or stimulus intensity to enable non-saturated recording

of the full-scale stimulus artifact. On the other hand, providing a low-impedance discharge path for the stimulation electrode using active feedback circuitry [18], [19], as well as careful design of the stimulator in terms of isolation of stimulation channels and parasitic current injection [20] have been previously shown to decrease the duration and amplitude of otherwise-saturating stimulus artifacts. But these approaches cannot fully eliminate the artifacts on their own, suggesting that an optimal solution might be to combine them with the subtraction techniques.

Since subtraction techniques typically require a DSP algorithm for the generation of the template signal, they have traditionally been implemented offline on a home-base computer post-data acquisition. To execute a subtraction-based SAR algorithm in real time (i.e., as the recording is taking place), a suitable template-generation technique should be selected and optimized, realized in hardware, and tested with real neural data, paving the way for ultimately implementing it on a custom integrated circuit (IC).

We have previously assessed the feasibility of hardware implementation of a subtraction-based SAR algorithm using the well-established finite impulse response (FIR) and infinite impulse response (IIR) temporal filtering techniques for template generation [21]. Using MATLAB$^{\text{TM}}$ simulations, both implementations were shown to be capable of removing stimulus artifacts upon reaching steady-state, with the IIR architecture offering a more favorable tradeoff among performance, computational resources, and power consumption at the expense of its operation speed.

This paper presents our work on hardware implementation of the IIR system proposed in [21] for a real-time SAR algorithm based on template subtraction. The paper is organized as follows. Section II describes the SAR algorithm and the corresponding IIR system architecture, and Section III analyzes its dynamic range and fraction length requirements to determine the number of bits for the internal nodes of the system in fixed-point computation. Section IV describes the implementation of the IIR SAR algorithm on a field-programmable gate array (FPGA), and Section V presents the measured FPGA results using two prerecorded neural datasets. Finally, Section VI draws some conclusions from this work.

II. SAR ALGORITHM

To generate a template signal representative of the stimulus artifact, temporal filtering is employed in which several properly shifted versions of the input neural data containing the stimulus artifacts are averaged. This is represented by [21]

$$y(t) = \sum_{n=0}^{N-1} a(n) \cdot x(t - nT_{sti}) \qquad (1)$$

where $y(t)$ is the estimated template signal, $x(t)$ is the input neural data containing the stimulus artifacts, N is the number of stimulus artifact waveforms used for template estimation, $a(n)$ are averaging factors that should sum up to unity for the stimulus artifact and $y(t)$ to have the same amplitude (e.g., $a(n)$ factors can be all equal to $1/N$ for standard averaging), and T_{sti} is the stimulation period. It should be noted that the stimulation
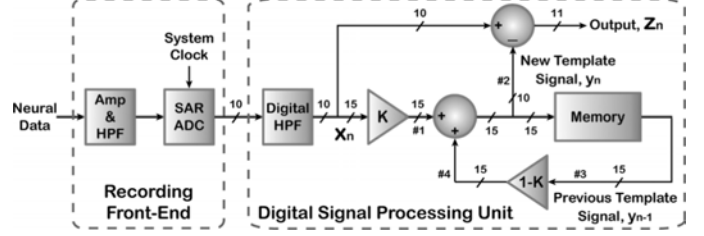

Fig. 1. System architecture for the IIR implementation of the template subtraction-based SAR algorithm. The number of bits in internal operation of the algorithm is also shown.

occurrence does not necessarily have to be periodic for correct operation of the SAR algorithm, as long as it is predictable via a stimulus timing signal.

An FIR implementation of (1) was previously shown to require at least $N - 1$ memory rows and N summations in each period of the sampling clock, whereas the IIR implementation would require a single memory row and only three summations at the expense of much longer system response time [21]. Initializing the memory with the first recorded artifact can significantly decrease the IIR system response time for creating an accurate artifact template signal [22]. Therefore, this paper focuses on the IIR implementation of the SAR algorithm with memory initialization.

Fig. 1 depicts the system architecture, comprising neural-recording front-end circuitry for signal conditioning and a DSP unit for executing the SAR algorithm. The recording front-end provides ac amplification, dc input stabilization, bandpass filtering, and 10b digitization of the recorded neural signal with fully programmable gain and bandwidth, similar to what has previously been shown in [3]. The DSP unit, which is the focus of this paper, provides additional highpass filtering using an IIR digital filter with adjustable bandwidth to remove any residual dc offsets or low-frequency noise, and performs real-time stimulus artifact rejection using template subtraction. Based on Fig. 1:

$$y_n = (1 - K) \cdot y_{n-1} + K \cdot x_n \qquad (2)$$

where y_n is the new artifact template signal, y_{n-1} is the previous template signal, and x_n is the input neural data. Therefore, in the IIR implementation, the stimulus artifact template signal is retained in the memory, and a new template signal is generated from the previous template signal and the input neural data according to (2), which is then subtracted from the input neural data. The factor K (<1) plays a similar role to N in (1), affecting the IIR system response time and accuracy. As shown in the Appendix, it can be derived from (2) that the minimum number of stimulus artifacts, m, required to generate an accurate template signal with error less than, e.g., 0.1% is

$$m > \frac{-3 - \log_{10}|1 - Y_0|}{\log_{10}(1 - K)} \qquad (3)$$

where Y_0 is the initial condition of the memory normalized to the steady-state artifact template signal. Fig. 2 shows a plot of m
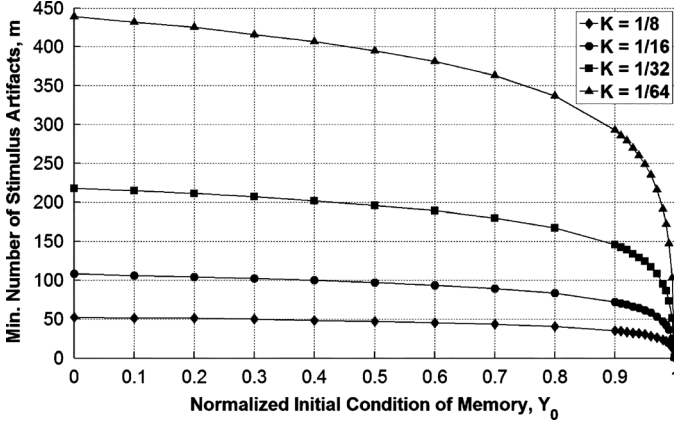
Fig. 2. Minimum number of stimulus artifacts required to generate an accurate template signal with error $<0.1\%$ as a function of the normalized initial condition of the memory ($Y_0 < 1$) for four different values of K.

Fig. 3. L1-norm estimates at nodes #1–4 for the two selected values of K.

versus Y_0 for four different values of K. Clearly, the closer the initial condition is to the steady-state template signal, the faster the system response time, showing that the IIR implementation is particularly effective when stimulus artifacts in consecutive stimulation cycles are reproducible. In this work, the factor K is selected to be either 1/16 or 1/32, which also allows implementing the multiplication-by-K function via a shift to the right by 4b or 5b, respectively, obviating the need for digital multipliers.

It is worth noting that the artifact template generation technique in (2) performed by the proposed IIR system is in essence an exponentially weighted moving average (EWMA) [23], a statistic tool with a rich history in process monitoring and quality control charting [24], [25] as well as economics [26] and industrial quality control [27]. In this paper, we utilize a real-time implementation of the EWMA for a novel application in neural signal processing. Section III discusses the performance of the IIR SAR algorithm with fixed-point computation and provides a framework for determining the optimum number of bits in internal operation of the algorithm.

III. SAR ALGORITHM WITH FIXED-POINT COMPUTATION

When template calculations are performed with floating-point precision, similar to when the SAR algorithm is executed offline in MATLAB$^{\mathrm{TM}}$ on a home-base computer post-data acquisition, the output can be very accurate. However, for *real-time* execution of the algorithm in hardware, fixed-point computation is preferred for simplicity, which then raises concerns about the template signal accuracy due to quantization noise. In this section, we find the optimum number of bits in internal operation of the SAR algorithm by analyzing the dynamic range and fraction length requirements.

In IIR systems, the internal nodes of the structure can potentially overflow, necessitating an adjustment in their dynamic range to satisfy the L1-norm criteria for preventing an overflow [28]–[30]. In Fig. 1, consider the signal path from the input neural data (i.e., x_n) to each of the four internal nodes of the algorithm (i.e., nodes #1–4). Assume the resulting transfer functions and corresponding impulse responses are $F_i(z)$ and $f_i[n]$,
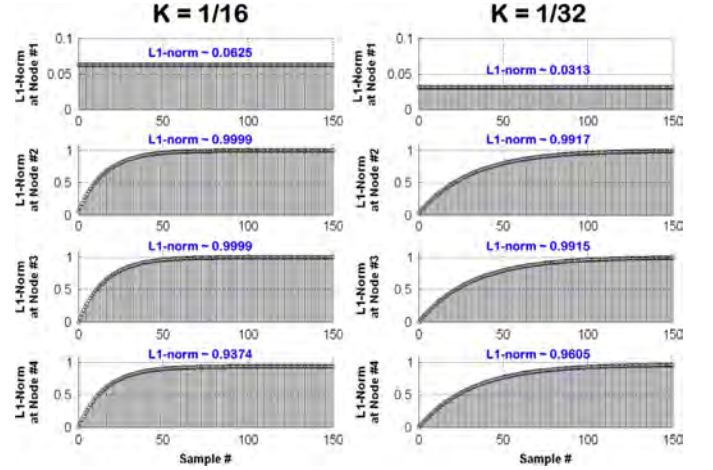
respectively. Modeling the memory block as a unit delay, it can be shown that

$$
\begin{aligned}
F_1(z) &= K \\
F_2(z) &= \frac{K}{1 - (1 - K)z^{-1}} \\
F_3(z) &= \frac{Kz^{-1}}{1 - (1 - K)z^{-1}} \\
F_4(z) &= \frac{K(1 - K)z^{-1}}{1 - (1 - K)z^{-1}}.
\end{aligned}
\tag{4}
$$

Fig. 3 depicts the L1-norm estimates of the four transfer functions for the two selected values of K, where L1-norm is

$$
\|f\|_1 = \sum_{n=0}^{\infty} |f[n]|.
\tag{5}
$$

As can be seen in all cases, the L1-norm estimates are less than one, indicating that no additional bits (equal to $\log_2 \|f\|_1$) are needed beyond 10b for the internal nodes to avoid overflow. The SAR algorithm output node ($z_n = x_n - y_n$) has higher dynamic range of 11b to prevent the saturation of the output after subtraction, in case of an overflow/underflow.

Next, to assess the impact of quantization noise induced by fixed-point computation on template signal accuracy, we determine the signal-to-noise ratio (SNR) in template signal generation as a function of the fraction length for the internal nodes (i.e., number of additional bits beyond 10b in a word-length). Fig. 4 shows the simulation structure for comparing the performance of the SAR algorithm with fixed-point computation versus that with floating-point computation by determining the SNR [31]. Q_1 and Q_2 are two quantizers that quantize their inputs to the word-length value, whereas Q_3 quantizes its input to 10b. Fig. 5 depicts the simulated SNR and effective number of
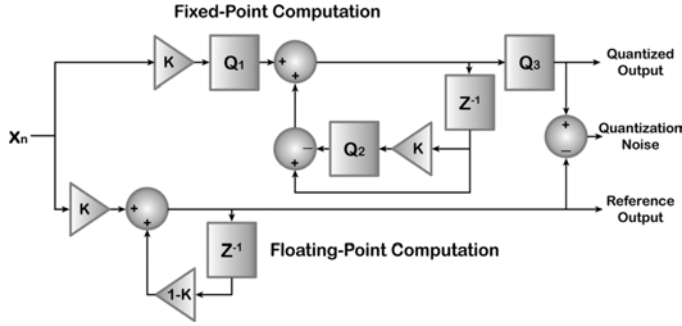
Fig. 4. Simulation structure for determining the SNR in template signal generation.
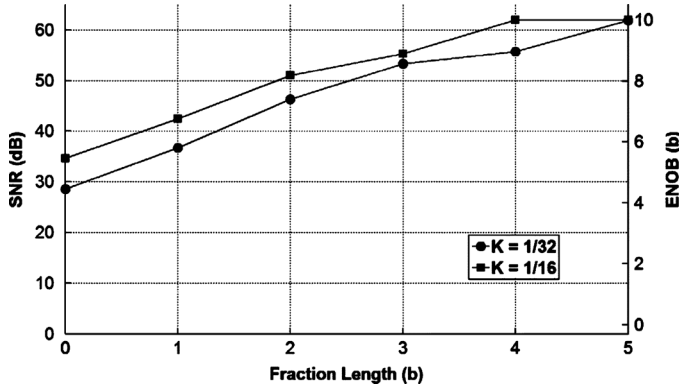

Fig. 5. Simulated SNR and ENOB of template signal generation in the IIR SAR algorithm with fixed-point computation versus the fraction length for the two selected values of K.

bits, ENOB, in template signal generation for the two selected values of K, where the SNR is defined as

$$\text{SNR} = 20 \log_{10} \frac{S_{\text{out,rms}}}{N_{Q,\text{rms}}} \tag{6}$$

with S_{out} and N_Q representing the reference output and quantization noise, respectively. Input x_n is taken to be a 10b-digitized sinusoidal signal with rail-to-rail amplitude (i.e., -512 to 511 in two's complement format) and a frequency of 0.1 mHz to capture the underlying assumption that the stimulus artifacts do not change rapidly with time. Assuming a stimulation frequency of 1 Hz, x_n's sampling frequency is also 1 Hz. Clearly, the system requires a fraction length of 5b to achieve ∼10b accuracy in template signal generation with $K = 1/32$. A lower fraction length would increase the quantization noise and degrade the accuracy to <10b, whereas a higher fraction length not only would increase the requisite hardware resources to support larger memory size, but also would not offer any significant benefit given that by design the overall system performance would be limited by that of the neural-recording front-end [3], and not the DSP unit. Taking into account these considerations related to dynamic range and fraction length requirements, the selected number of bits for the internal operation of the SAR algorithm is shown in Fig. 1.

IV. FPGA Implementation

The DSP unit in Fig. 1, comprising the digital highpass filter (HPF) and the SAR algorithm circuitry, has been implemented on an FPGA using the DE2 Development and Educational Board, which has the Cyclone II device by *Altera* as its FPGA platform. Fig. 6 depicts the architecture of the DSP unit in FPGA implementation, which incorporates a 68b parameter register, a digital control unit, and a DSP core. The parameter register is used to store the user-selectable parameters for system operation such as the bandwidth setting of the digital HPF and factor K in the SAR algorithm, as well as memory initialization, memory length, and output-blanking settings. The memory length (i.e., number of 16b samples) is determined by the sampling clock frequency and the stimulus artifact duration. If needed, the blanking feature is used after template subtraction to remove any residual artifacts in the output around the rising and falling edges of the artifact where it rapidly changes with time [21]. The parameter register is implemented as a standalone circuit block with its own timing and control operation, which is separate from that of the other circuit blocks and applied externally. This is because this block is loaded with the requisite system parameters only once prior to the experiment and is not synchronously clocked with the rest of the circuit during SAR algorithm operation.

The digital control unit incorporates counters and finite-state machines and provides timing, path, and blanking control signals for the DSP core. The required inputs for the digital control unit include a stimulus timing signal, system clock and sampling clock signals, and system parameters such as memory length, memory initialization, and blanking settings.

The DSP core incorporates a digital HPF, circuitry to execute the SAR algorithm, and parallel-to-serial converters at the output. The required inputs for the DSP core include the amplified/digitized neural signal (10b), system clock signal, and control signals provided by the digital control unit. Fig. 6 also shows the structure of the digital HPF and SAR algorithm circuitry in the DSP core as implemented on the FPGA. The amplified/digitized input neural signal is first highpass filtered using a 1st-order, IIR filter with direct form II architecture. Factor K_1 is the user-selected HPF coefficient that controls the filter bandwidth and is selected judiciously to perform the filtering using arithmetic shifts, subtraction and addition only, with no need for digital multipliers or dividers [3]. The user can set K_1 to be either 1/16 or 1/8, which results in a filter cutoff frequency of 366 Hz or 756 Hz, respectively, from a 1-MHz system clock. Since the digitized data at the analog-to-digital converter (ADC) output are unsigned numbers (10b), a factor of 512 is subtracted from the input signal to convert it to two's complement format for further processing. In addition, an overflow/underflow detector is used at the HPF output to limit its dynamic range to 10b before feeding it to the SAR algorithm circuitry.

The SAR algorithm only operates for the duration of each stimulus artifact. The digitized/filtered sample at the output of the HPF filter (10b) is first converted to 15b via a shift to the left by 5b and then multiplied by factor K_2 (same as K in Fig. 1) stored in the parameter register. Next, the memory data containing the previous template signal are read, multiplied by
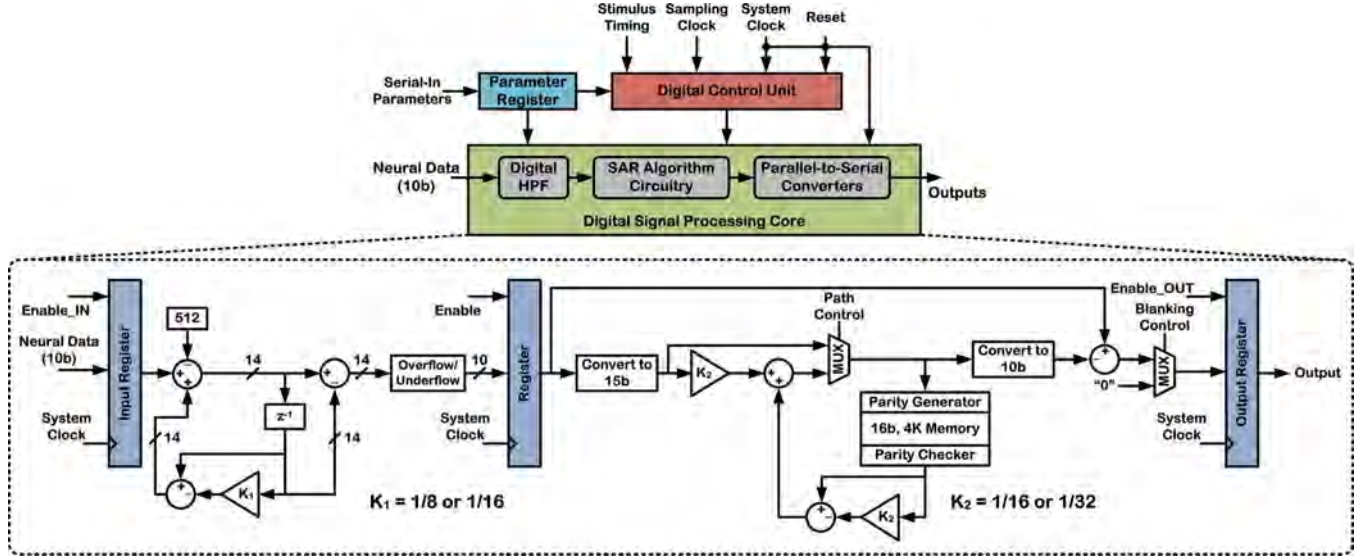
Fig. 6. Architecture of the DSP unit (top) and structure of the digital HPF and SAR algorithm circuitry in the DSP core (bottom) as implemented on the FPGA.

$(1 - K_2)$, and added to $(K_2 \cdot x_n)$ to obtain the new template signal (15b), which is written back into the memory for the next cycle. The new template signal is also converted back to 10b and subsequently subtracted from the 10b digitized/filtered input sample to produce the SAR algorithm output signal. Outside the duration of the stimulus artifact, the SAR algorithm circuitry is disabled and the digitized/filtered sample at the HPF output is directly passed to the output register.

The path control signal from the digital control unit manages the memory initialization. Specifically, if the recorded stimulus artifact is the first artifact, indicated as such by the stimulus timing signal, the path control signal routes the 15b sample directly to the memory input for its initialization. With the next indication of stimulation by the stimulus timing signal, the IIR system executes the SAR algorithm as previously described. If the memory initialization setting is not enabled by the user, the memory can be cleared to start with zero internal values, but this would increase the IIR system response time as previously shown in Fig. 2.

The 16b, 4K memory is implemented using the internal SRAM of the FPGA. Even parity is used to check for memory error, which is generated by an *XOR* function of all the bits in each 15b sample. The parity bit is then added to the end of the data bits before being written into the memory as a 16b sample. When the memory data are read out, a parity checker checks for memory error, and this information is sent to the output. The 15b sample is also sent to the rest of the SAR algorithm circuitry for template generation. Including the memory parity check feature, while not entirely necessary for an FPGA-based system, would streamline the design translation from an FPGA to an IC platform in the future.

The blanking control signal, which is also received from the digital control unit, is used to remove any residual artifacts in the output after template subtraction. Specifically, this control signal activates a multiplexer that replaces the output data with "0" for the time period in which blanking is applied, which is normally at the rising and falling edges of the artifact where it

rapidly changes with time. The user can independently set the blanking duration around the rising and falling edges from 0 (i.e., no blanking) to 2,047 data points.

The three registers in Fig. 6 are used for pipelining in order to overlap the processing in each stage and prevent harmful race conditions with proper timing control. Further, since the SAR algorithm circuitry operates synchronously with a system clock, all circuit blocks (except the parameter register) share the same system clock signal globally and use a local *Enable* signal for synchronization [32].

V. FPGA MEASUREMENT RESULTS

The DSP unit as depicted in Fig. 6 has been synthesized and mapped to the Cyclone II FPGA, EP2C35F672C6, using *Altera*'s Quartus II design software. The mapped circuitry consumed 2% (656) of the total available logic elements (LEs) and 14% (65,536) of the total available memory bits. The DE2 board was programmed and connected to a digital data acquisition (DAQ) card, NI 6541, which provided the input signal to the FPGA and recorded the output waveforms. The system clock was applied to the FPGA using the onboard external clock port, and a supply of 9 V was used to power up the board with its input-output (I/O) ports at 3.3 V. For all FPGA measurements described below, factors K_1 and K_2 (see Fig. 6) were both set to 1/16.

Two sets of prerecorded neural data from two different laboratories were used to experimentally verify the operation of the IIR SAR algorithm and its FPGA implementation. Specifically, a 294-s window of prerecorded neural data from a rat was used as the first dataset. The rat data were sampled at ~24.4 kHz and obtained during 4-Hz cortical stimulation. A gain of 520 (~54.3 dB) was applied to the neural data before feeding it to the FPGA. The SAR algorithm was set to operate for 5 ms upon receiving an indication of stimulation by the stimulus timing signal, and no output blanking was applied.

A 125-s window of prerecorded data from an *Aplysia californica* (a marine sea slug) was used as the second neural dataset.
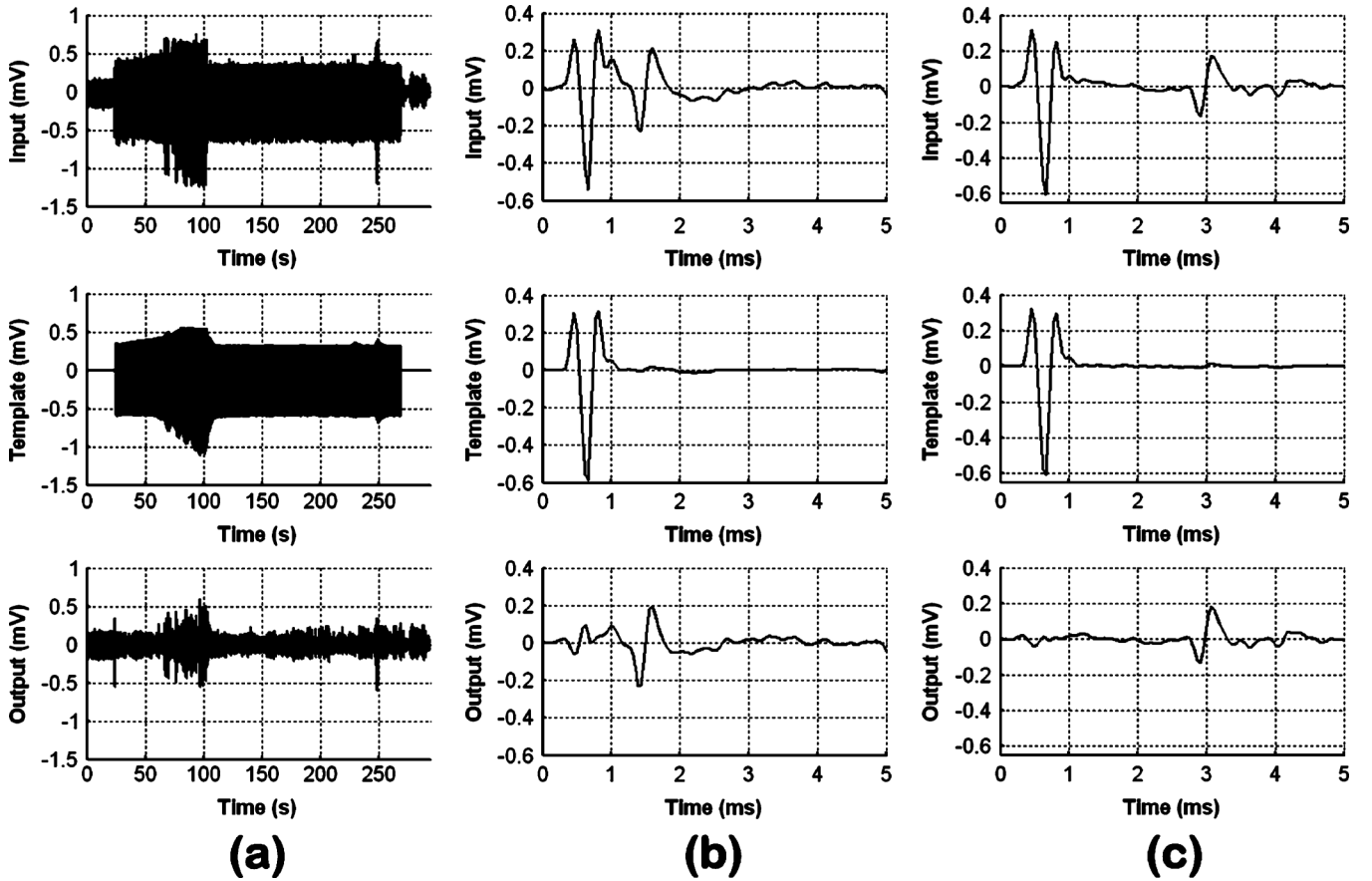
Fig. 7. FPGA measurement results using prerecorded neural data from a laboratory rat. (a) Top plot shows a 294-s window of the input data to the FPGA. Middle plot depicts the generated stimulus artifact template signal, whereas the bottom plot shows the IIR system output from the FPGA. Two 5-ms snapshots of the waveforms are shown at (b) t $=\sim$ 208 s and (c) t $=\sim$ 256 s.

The *Aplysia* data were sampled at 2 kHz and obtained during 0.5-Hz stimulation. A gain of 1,000 (60 dB) was applied to the neural data before feeding it to the FPGA. Upon receiving an indication of stimulation by the stimulus timing signal, the SAR algorithm was set to operate for 96 ms (the duration of stimulus artifact in the *Aplysia* dataset was much longer than that in the rat dataset), and output blanking was set to occur for 4 ms synchronized with the rising and falling edges of the stimulus timing signal. The applied gain values represented those previously obtained with our neural-recording front-end operating from 1.5 V [3]. The gain values were high enough to achieve sufficient resolution at the DSP unit input, while keeping the amplitude of the amplified neural data below 1.5 V_{pp}.

Fig. 7 shows the FPGA measurement results using the rat neural dataset. The top plot in (a) depicts the input neural data to the FPGA, consisting of neural spikes buried in large stimulus artifacts. The middle plot shows the generated artifact template signal after memory initialization as previously described. Note the fast response time of the IIR SAR algorithm in quickly generating the template signal even for the initial stimulus artifacts, as well as how fast the generated template signal tracks the variation in stimulus artifact amplitude in the first 100 seconds. The bottom plot depicts the IIR system output from the FPGA in which the large stimulus artifacts are rejected and the neural data recovered in real time.

Fig. 7(b) and (c) depict 5-ms snapshots of the waveforms at t = $\sim$208 s and $\sim$256 s, respectively, demonstrating that the system is fully capable of recovering neural action potentials that occur on the tail end of the artifact [see Fig. 7(c)] or appear as close as within 0.5 ms after the artifact spike [see Fig. 7(b)].

The slight discrepancy between the amplitude of the input artifact and that of the template signal is because the template signal actually represents the highpass filtered artifact.

Fig. 8 shows a 5-s snapshot of the waveforms in Fig. 7(a) around the onset of stimulation and their corresponding spectrograms obtained using 1,024-sample windows with 1,000-sample overlap. As can be seen in the top and middle spectrograms, the artifacts in the rat neural dataset have strong frequency components below 5 kHz that are significantly reduced in the output (see the bottom spectrogram), allowing the weaker neural activity to emerge from the large artifacts. For the very first stimulus artifact at just prior to t = 2.5 s, which is the one loaded into the memory for its initialization, the corresponding template signal would be 1/16th of the artifact according to (2), and therefore 15/16th of the artifact appears in the output data after subtraction. The IIR SAR algorithm then removes all the subsequent stimulus artifacts starting with the second one. If present, artifact residuals as seen in Figs. 7(b) and (c) in the time domain and Fig. 8 in the frequency domain (bottom spectrogram) are now insignificant as compared to the neural action potentials.
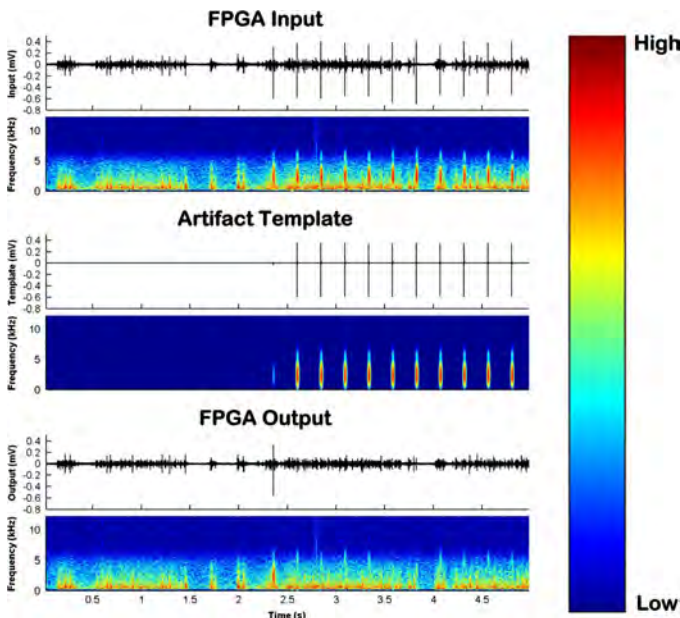
Fig. 8. A 5-s snapshot of the FPGA measurement results using the prerecorded rat neural dataset and their corresponding spectrograms. The 5-s snapshot is taken around the stimulus onset.
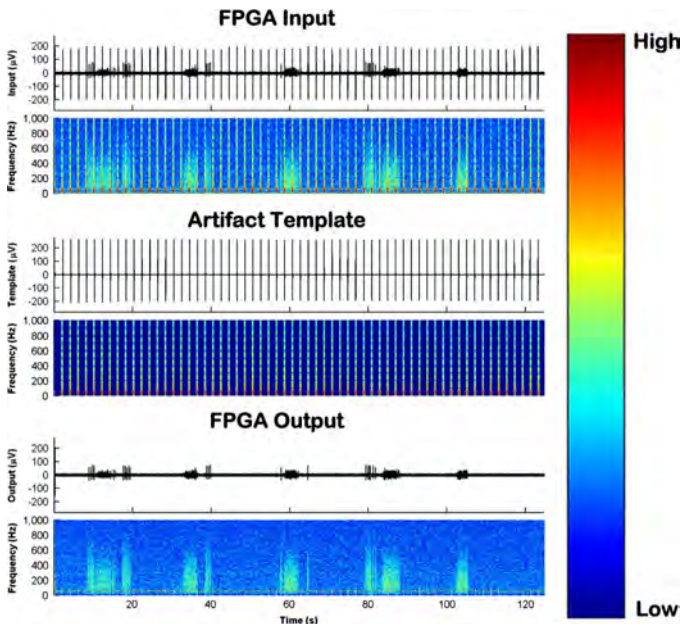

Fig. 9. FPGA measurement results using the prerecorded *Aplysia* neural dataset and their corresponding spectrograms.

Fig. 9 shows the FPGA measurement results using the *Aplysia* neural dataset and their corresponding spectrograms. The top plot depicts the input neural data to the FPGA, containing many large stimulus artifacts that occur at 0.5 Hz and bursts of extracellular neural activity that occur in between and occasionally on the tail end of the artifacts. The middle plot shows the generated artifact template signal and its spectrogram, indicating that the artifacts have their frequency components spread throughout a 1-kHz bandwidth with strong frequency components contained below 200 Hz. The bottom plot shows the FPGA output data after blanking in which all
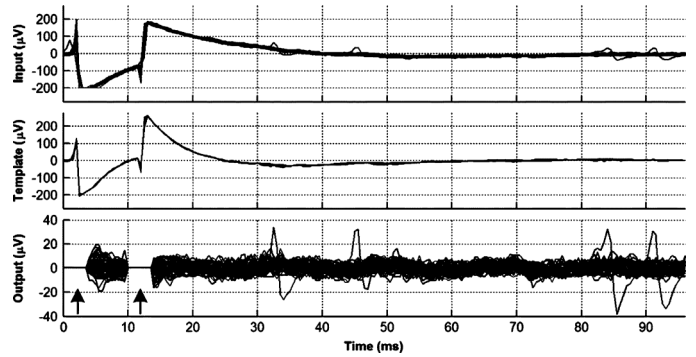

Fig. 10. Top plot shows a 96-ms portion of the *Aplysia* neural dataset, showing a total of 61 unfiltered stimulus artifacts superimposed on each other with some action potentials riding on the tail end of the artifacts. Middle plot depicts the 61 stimulus artifact templates superimposed on each other, which actually represent the highpass filtered artifacts (not shown). Bottom plot shows the artifact-free FPGA output in which the neural spikes are recovered after template subtraction. Residual artifacts are also simultaneously removed after 4-ms blanking (arrows). Note the smaller dynamic range of the Y-axis in the bottom plot after artifact removal and residual blanking.

stimulus artifacts (minus the first one as explained previously) are successfully removed from the recorded data in real time to recover the neural activity.

Fig. 10 shows a close-up view of the waveforms during the 96-ms period of operation for the SAR algorithm. The top plot depicts 61 unfiltered stimulus artifacts superimposed on each other (i.e., all the artifacts present in the 125-s window of *Aplysia* neural dataset minus the very first one), with some action potentials also occurring on the tail end of the artifacts. The middle plot shows the corresponding artifact templates superimposed on each other, whereas the bottom plot depicts the artifact-free IIR system output from the FPGA after template subtraction and 4-ms blanking (arrows) for simultaneous removal of the artifacts and artifact residuals, respectively, demonstrating successful operation of the algorithm and its hardware implementation.

In order to assess the performance of the IIR SAR algorithm and its hardware implementation in a quantitative manner, a total of 908 stimulus artifacts (54 of 62 and 854 of 1,000 artifacts in the *Aplysia* and rat neural datasets, respectively) were analyzed. Specifically, the mean and standard deviation of the root-mean-square (rms) values of the artifacts were computed pre- and post-processing by the FPGA.

The analysis excluded the very first artifact in each neural dataset and those artifacts that had action potentials present anywhere in their duration over which the algorithm was operating (96 ms and 5 ms for the *Aplysia* and rat artifacts, respectively). This ensured that the occasional presence of action potentials did not confound the analysis. The same statistics were also obtained from segments of the FPGA output that represented pure noise (i.e., absence of both action potentials and artifact residuals). Table I tabulates the results of this analysis. In the case of *Aplysia* neural dataset that contains relatively stationary stimulus artifacts (see the top plot in Fig. 9 and note the small standard deviation value in Table I), the rms value of the artifact on average is reduced by a factor of 17, resulting in post-processed rms values that are at the level of that for the output

TABLE I
STATISTICS OF PRE- AND POST-PROCESSED STIMULUS ARTIFACTS

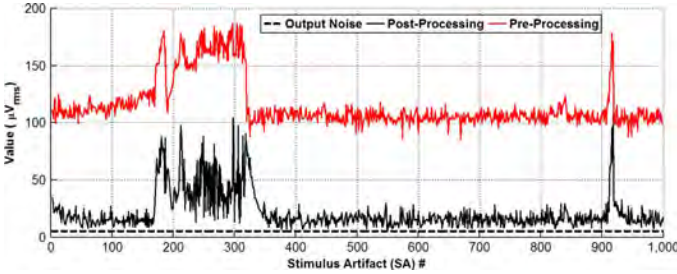| *Aplysia californica (54 of 62 SAs)*		
	Mean (μV_{rms})	SD (μV_{rms})
Pre-Processing	68.33	1.21
Post-Processing	4.01	0.68
Output Noise	3.83	0.16
Rat (854 of 1,000 SAs)		
Pre-Processing	115.74	21.72
Post-Processing	21.65	16.70
Output Noise	5.03	0.46

Fig. 11. Root-mean-square (rms) value of the stimulus artifacts (854 of 1,000) in the rat neural dataset pre- and post-processing by the FPGA. The dashed line represents an average rms value of 5.03 μV for the output noise obtained from 10 different 5-ms segments that did not contain any action potentials or artifact residuals.

noise. In the case of rat neural dataset that contains both stationary and non-stationary artifacts (see the top plot in Fig. 7(a) and note the larger standard deviation value in Table I), the reduction in the rms value on average is more modest (a factor of 5.3). A closer look at the rms values of individual stimulus artifacts pre- and post-processing reveals that the degradation of performance is limited to when there is a sudden change in the artifacts (see Fig. 11 and compare its trend with how the artifacts are changing in the top plot of Fig. 7(a)), whereas the rms values of the post-processed artifacts indeed approach that of the output noise when the artifacts are relatively stationary.

VI. CONCLUSION

This paper reported on a neural signal-processing algorithm for real-time stimulus artifact rejection (SAR) in which a high-fidelity template signal representative of the stimulus artifacts was first generated via temporal filtering and subsequently subtracted from the contaminated neural data to remove the artifacts. A system architecture for the IIR implementation of the algorithm was realized in hardware on an FPGA platform, featuring memory initialization as a simple method to significantly decrease the IIR system response time for accurate template generation. The measured FPGA results using two sets of prerecorded neural data from a rat and an *Aplysia californica* verified the functionality of the algorithm and its hardware implementation by removing the stimulus artifacts in real time from the contaminated recorded data and recovering the extracellular neural activity.

The major advantage of this approach as compared to the blanking techniques (i.e., disconnecting the recording amplifier

input during stimulation) is that it has the potential to retain signal information during stimulation while fully eliminating the artifacts from the contaminated data record in real time. On the other hand, one limitation of this approach is that it does not directly address the problem of amplifier saturation and hence becomes less effective with prolonged amplifier saturation, unless care is taken in the design of the recording and stimulating circuitry to prevent (or at least minimize) amplifier saturation by decreasing the duration and amplitude of the artifacts [18]–[20]. Another limitation of this approach is that if neural activity occurs on the tail end of the artifact and is time-locked to stimulation, it will be removed by the system along with the artifacts. Similarly, if neural activity occurs during the rising/falling edges of the artifact spike, it will be lost, because it will be either blanked out by the system or heavily distorted by the residuals with no blanking.

This technique can potentially handle other stimulation scenarios as well, given that it only needs the stimulus timing signal information for correct operation. For example, if stimulation occurs *simultaneously* on two electrodes, a *combined* stimulus artifact might appear on the recording electrode that can be removed even by the current system. If stimulation occurs *alternately* on two electrodes, two different stimulus artifact types might appear *alternately* as well on the recording electrode and can be removed by modifying the timing operation of the system to handle each artifact type independently, if there is no temporal overlap between the artifacts. Ultimately, a tradeoff exists between functional versatility and system operation complexity.

Finally, given the relatively low system clock frequency of ≤ 1 MHz in this work and that the synthesized algorithm utilized a very small percentage of the available FPGA resources, it was not readily feasible to accurately determine the power consumption in hardware implementation. Efforts are currently under way for custom implementation of the DSP unit in Fig. 1 on an IC that would also incorporate recording front-end and stimulating back-end circuitry adapted from [3] to form a complete system. To that end, our preliminary work shows that the DSP unit can be implemented with a total area of 3.64 mm^2 (89% occupied by the 16b, 4K SRAM) in 0.35-μm CMOS technology with power consumption on the order of low-tens of microwatts from 1.5 V (1-MHz system clock), indicating the feasibility of running the algorithm on a miniaturized, integrated device in the near future.

APPENDIX

In this Appendix, we show the derivation of (3) in Section II: SAR Algorithm. As previously stated, based on Fig. 1

$$y_n = (1 - K) \cdot y_{n-1} + K \cdot x_n \qquad (A1)$$

where n $= 1, 2, 3, \dots$. Hence, it is simple to see that

$$\begin{aligned}
y_1 &= (1 - K) \cdot y_0 + K \cdot x_1 \\
y_2 &= (1 - K) \cdot y_1 + K \cdot x_2 \\
&= (1 - K)^2 \cdot y_0 + K \cdot (1 - K) \cdot x_1 + K \cdot x_2 \quad (A2)
\end{aligned}$$

which means that the template signal for the mth artifact can be written as

$$y_m = (1 - K)^m \cdot y_0 + K \cdot [x_m + (1 - K) \cdot x_{m-1} + \cdots + (1 - K)^{m-1} \cdot x_1] \quad (A3)$$

where y_0 is the initial condition of the memory. Assume that $x_1, x_2, \ldots x_m$ are all equal to the steady-state artifact template signal, y_{ss}. Therefore

$$\frac{y_m}{y_{ss}} = (1-K)^m \cdot Y_0 + K \cdot [1 + (1-K) + \cdots + (1-K)^{m-1}] \quad (A4)$$

where $Y_0 = (y_0)/(y_{ss})$ is the initial condition of the memory normalized to the steady-state artifact template signal. Given the sum of geometric series, it can be shown that

$$1 + (1 - K) + \cdots + (1 - K)^{m-1}$$
$$= \frac{1 - (1 - K)^m}{1 - (1 - K)}$$
$$= \frac{1 - (1 - K)^m}{K} \quad (A5)$$

which means that (A4) can be simplified to

$$\frac{y_m}{y_{ss}} = (1 - K)^m \cdot Y_0 + 1 - (1 - K)^m. \quad (A6)$$

If $Y_0 < 1$, for generating an accurate template signal with error less than, e.g., 0.1%, one needs to have $(y_m)/(y_{ss}) > 0.999$, which means $(1 - K)^m \cdot (1 - Y_0) < 0.001$ from (A6). Taking a logarithm of both sides and noting that $\log_{10}(1 - K) < 0$, one can obtain

$$m > \frac{-3 - \log_{10}(1 - Y_0)}{\log_{10}(1 - K)}. \quad (A7)$$

If $Y_0 > 1$, for generating an accurate template signal with error less than 0.1%, one needs to have $(y_m)/(y_{ss}) < 1.001$, which ultimately leads to

$$m > \frac{-3 - \log_{10}(Y_0 - 1)}{\log_{10}(1 - K)}. \quad (A8)$$

ACKNOWLEDGMENT

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Appendix III   D. J. Guggenmos, M. Azin, S. Barbay, J. D. Mahnken, C. Dunham, P. Mohseni, and R. J. Nudo, "Restoration of function after brain damage using a neural prosthesis," *Proc. Natl. Acad. Sci. USA (PNAS)*, vol. 110, no. 52, pp. 21177-21182, December 2013.

Restoration of function after brain damage using a neural prosthesis

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Neural interface systems are becoming increasingly more feasible for brain repair strategies. This paper tests the hypothesis that recovery after brain injury can be facilitated by a neural prosthesis serving as a communication link between distant locations in the cerebral cortex. The primary motor area in the cerebral cortex was injured in a rat model of focal brain injury, disrupting communication between motor and somatosensory areas and resulting in impaired reaching and grasping abilities. After implantation of microelectrodes in cerebral cortex, a neural prosthesis discriminated action potentials (spikes) in premotor cortex that triggered electrical stimulation in somatosensory cortex continuously over subsequent weeks. Within 1 wk, while receiving spike-triggered stimulation, rats showed substantially improved reaching and grasping functions that were indistinguishable from prelesion levels by 2 wk. Post hoc analysis of the spikes evoked by the stimulation provides compelling evidence that the neural prosthesis enhanced functional connectivity between the two target areas. This proof-of-concept study demonstrates that neural interface systems can be used effectively to bridge damaged neural pathways functionally and promote recovery after brain injury.

brain–machine–brain interface | neural plasticity | traumatic brain injury | closed-loop | long-term potentiation

The view of the brain as a collection of independent anatomical modules, each with discrete functions, is currently undergoing radical change. New evidence from neurophysiological and neuroanatomical experiments in animals, as well as neuroimaging studies in humans, now suggests that normal brain function can be best appreciated in the context of the complex arrangements of functional and structural interconnections among brain areas. Although mechanistic details are still under refinement, synchronous discharge of neurons in widespread areas of the cerebral cortex appears to be an emergent property of neuronal networks that functionally couple remote locations (1). It is now recognized that not only are discrete regions of the brain damaged in injury or disease but, perhaps more importantly, the interconnections among uninjured areas are disrupted, potentially leading to many of the functional impairments that persist after brain injury (2). Likewise, plasticity of brain interconnections may partially underlie recovery of function after injury (3).

Technological efforts to restore brain function after injury have focused primarily on modulating the excitability of focal regions in uninjured parts of the brain (4). Purportedly, increasing the excitability of neurons involved in adaptive plasticity expands the neural substrate potentially involved in functional recovery. However, no methods are yet available to alter the functional connectivity between spared brain regions directly, with the intent to restore normal communication patterns. The present paper tests the hypothesis that an artificial communication link between uninjured regions of the cerebral cortex can restore function in a rodent model of traumatic brain injury (TBI). Development of such neuroprosthetic approaches to brain repair may have important implications for the millions of individuals who are left with permanent motor and cognitive impairments after acquired brain injury, as occurs in stroke and trauma.

For the present experiment, we used a rodent model of focal brain injury to the caudal forelimb area (CFA), a region that is part of the cortical sensorimotor system. This area in the frontal cortex shares many properties with primary motor cortex (M1) of primates; injury to M1 results in long-term impairment in reaching and grasping functions (5). Traditionally, it has been thought that impairment occurs because M1 provides substantial outputs to the motor apparatus in the spinal cord, thus directly affecting motor output function. However, M1 also has important interconnections with the primary somatosensory cortex (S1) located in the parietal lobe (Fig. 1A). Long-range corticocortical fibers from S1 provide critical information to M1 about the position of the limb in space. Thus, injury to M1 results in impaired motor performance due, at least in part, to disruption in communication between the somatosensory and motor cortex (6).

To test our hypothesis that functional recovery can be facilitated by creating an artificial communication link between spared somatosensory and motor regions of the brain, we focused on the rat's premotor cortex (PM). The rostral forelimb area (RFA) is a premotor area in the rodent's frontal cortex that shares many properties with PM of primates and is thought to participate in recovery of function after injury to M1 (5, 7–9). PM areas are so-named because the principal target of their output fibers is M1 (10). PM areas also have long-range corticocortical connections with somatosensory areas, but at least in

Significance

Closed-loop systems, or brain–machine–brain interfaces (BMBIs), have not been widely developed for brain repair. In this study, we targeted spared motor and somatosensory regions of the rat brain after traumatic brain injury for establishment of a functional bridge using a battery-powered microdevice. The results show that by using discriminated action potentials as a trigger for stimulating a distant cortical location, rapid recovery of fine motor skills is facilitated. This study provides strong evidence that BMBIs can be used to bridge damaged neural pathways functionally and promote recovery after brain injury. Although this study is restricted to a rodent model of TBI, it is likely that the approach will also be applicable to other types of acquired brain injuries.
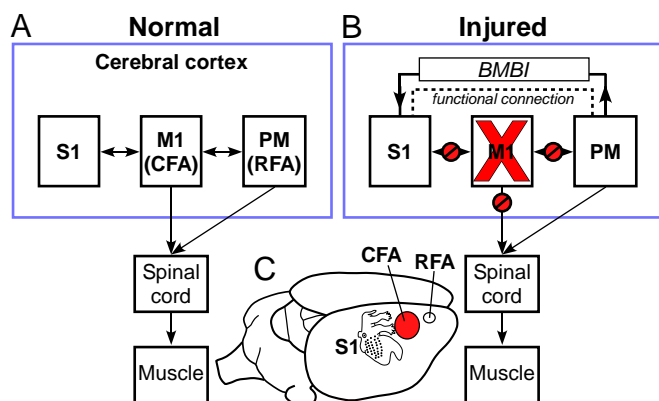
NEUROSCIENCE

Fig. 1. Theoretical model of neuroprosthetic treatment approach after brain injury. (*A*) Normal connectivity of M1, S1, and PM. Both M1 (CFA in rat) and PM (RFA in rat) send substantial outputs to the spinal cord via the corticospinal tract. Also, extensive reciprocal connections exist between M1 and PM, as well as between M1 and S1. (*B*) Effects of focal M1 injury on brain connectivity and the hypothetical effect of a BMBI to restore somatosensory-motor communication. An injury to M1, as might occur in stroke or brain trauma, results in a focal area of necrosis, as well as loss of M1 outputs to the spinal cord. Corticocortical communication between M1 and S1 (and between M1 and PM) is also disrupted, further contributing to functional impairment. Because the uninjured PM also contains corticospinal neurons, it might have the ability to serve in a vicarious role. The dotted line indicates enhanced functional connection between PM and S1 that we propose is established after treatment with a BMBI. (*C*) Location of target areas in rat cerebral cortex. A topographic map of the somatosensory representation in S1 is superimposed on the cortex.

intact animals, they appear to be relatively weak compared with M1's connections with the somatosensory cortex (9, 11, 12).

Our approach was to link the neural activity of the PM forelimb area (RFA) functionally with activation of the S1 forelimb area following a controlled cortical impact (CCI) to M1 (Fig. 1 *B* and *C*). To this end, a microdevice was developed with the ability to deliver activity-dependent stimulation (ADS) through recording and digitizing extracellular neural activity from an implanted microelectrode, discriminating individual action potentials (spikes), and delivering small amounts of electrical current to another microelectrode implanted in a distant population of neurons (13, 14). This closed-loop system was similar, in principle, to the "Neurochip" used previously by other investigators to demonstrate the effects of local ADS in intact animals (15), but it was miniaturized for head-mounted, wireless operation (Fig. 2*A* and Fig. S1). By linking the activity of one area of the cortex with that of a distant area of the cortex, a closed-loop brain–machine–brain interface (BMBI) for artificial corticocortical communication between PM and S1 was created.

Individual spikes were detected in PM, and subsequent stimulation was delivered to S1 after a 7.5-ms delay (Fig. 2*B*). (Because connections between distant cortical areas are commonly reciprocal, enhanced communication theoretically could be established by ADS in either direction.) After the M1 injury, rats were implanted with microelectrodes connected to the BMBI microdevice (Fig. 2*A*). The microdevice delivered ADS 24 h per day up to 28 d postinjury, except for brief motor assessment sessions on predetermined days. Behavioral recovery in ADS rats was compared with recovery in rats with open-loop stimulation (OLS), in which S1 stimulation was uncorrelated with spikes in PM, and with control rats that had no microdevice implanted.

Results

Testing Motor Skill After Brain Injury. The primary behavioral assay for determining whether ADS resulted in functional improvement

after brain injury was a skilled reaching task. This widely used task is a particularly sensitive measure of forelimb motor function after M1 lesions in both rodents and primates. Rats were pretrained to achieve a minimum criterion score of >70% successful pellet retrievals. After the lesion was created, rats were tested on the task during assessment sessions on postlesion days 3, 5, 8, 14, 21, and 28. During each postlesion assessment session, rats were tested under two conditions: first with the microdevice stimulation function turned OFF and then with the stimulation function turned ON. Rats in each of the three groups demonstrated a severe deficit on the skilled reaching task in the first few days after the injury (Fig. 3). On postlesion days 3 and 5, there were no significant differences in motor performance between the groups (global comparisons: $P = 0.5265$ and $P = 0.0945$, respectively). Rats in the control group (with a lesion but no microdevice) continued to demonstrate a profound deficit that plateaued at only about 25% successful retrievals. In striking contrast, by postlesion day 8, group performance was significantly different (global comparison: $P = 0.0044$). Rats in the ADS group showed a substantial and statistically significant behavioral improvement in reaching success compared with rats in the other groups in the ON condition (pairwise comparisons: $P = 0.0418$ for ADS vs. OLS, $P = 0.0012$ for ADS vs. control, and $P = 0.2110$ for OLS vs. control; Fig. 3 and Movies S1 and S2). By postlesion day 14, the performance of the rats in the ADS group was approximately at prelesion levels and significantly higher than that of rats in the other groups. The difference between the OLS group and the control group approached significance on day 14 (global comparison: $P = 0.0004$; pairwise comparisons: $P = 0.0284$ for ADS vs. OLS, $P < 0.0001$ for ADS vs. control, and $P = 0.0555$ for OLS vs. control). By postlesion day 21, performance in the ADS group remained high and statistically different from that of the control group. Performance was not significantly different in the ADS group between days 14 and 21 ($P = 0.576$). However, by day 21, the OLS group had improved further, so that the difference between the two groups was not significant (global comparison: $P = 0.0007$;
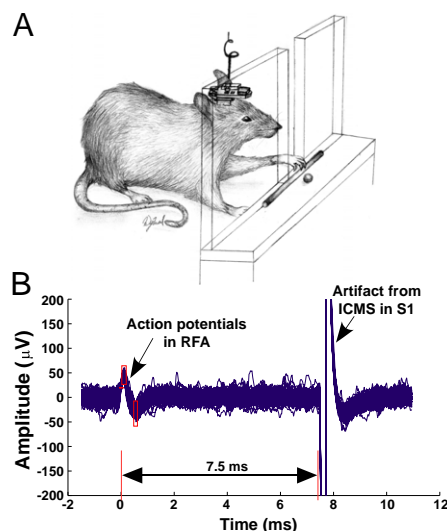
Fig. 2. ADS protocol. After injury to the CFA, a recording microelectrode was placed in the RFA, whereas a stimulating microelectrode was placed in the distal forelimb field of S1. A BMBI discriminated action potentials in the RFA, and after a 7.5-ms delay, it delivered a low-level electrical current pulse to S1 (13). (*A*) Sketch of a rat retrieving a food pellet with a BMBI attached to the skull. (*B*) Sample traces of recordings from the RFA showing action potentials and stimulus artifacts from an ICMS current delivered to S1. Time-amplitude window discriminators are indicated by red boxes. A total of 100 superimposed traces are shown.

Fig. 3. Performance of rats on a skilled reaching task after injury to M1 (ON condition). The ADS group is shown in red, the 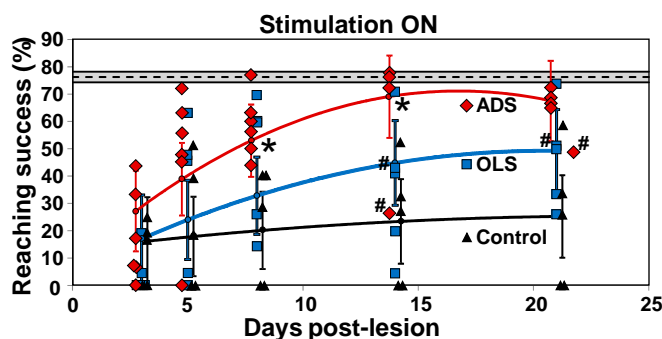OLS group is shown in blue, and the control group is shown in black. The dotted line indicates the average prelesion performance of all animals in the study. The bounded area indicates the 95% confidence interval. Regression lines are based on an LMM (43). Error bars represent 95% confidence intervals. *$P < 0.05$ (pairwise difference between the ADS and OLS groups). Because the statistical analysis was an intent-to-treat model, rats were included in the analysis even if the microdevice was no longer functional. Only one rat in the ADS group had a microdevice that was functional by postlesion day 28; thus, figures are presented through postlesion day 21 (*SI Results*). Diamonds, squares, and triangles represent individual animal data points. #, microdevice not functional (Tables S1 and S2).

pairwise comparisons: $P = 0.0891$ for ADS vs. OLS, $P = 0.0002$ for ADS vs. control, and $P = 0.0278$ for OLS vs. control). Although the mean performance of the ADS group was higher than that of the OLS group even in the OFF condition, differences were not statistically significant on any postlesion day (Fig. S2).

Immediate Effects Within Single Sessions. Rats in the ADS group often showed substantially improved performance within a single day's session when the microdevice was switched from the OFF to the ON condition. One particularly salient example can be seen in a video of a rat in the ADS group on postlesion day 8 (Movie S2). In the OFF condition, this rat made many attempts to reach through the opening in the Plexiglas but was rarely able to do so accurately. Large trajectory errors were made, and relatively few retrievals were completed successfully. Following completion of trials in the OFF condition, the microdevice was programmed to the ON state, a process that required 2–3 min. As soon as the microdevice was turned ON, the rat began to retrieve pellets with noticeably enhanced success. Movements tended to be slower and seemingly more deliberate, and fewer errors were made. A statistical analysis of the ADS group between the OFF and ON conditions revealed significantly better performance in the ON condition on postlesion day 3 ($P = 0.0003$), postlesion day 5 ($P = 0.0005$), and postlesion day 8 ($P = 0.0019$) and marginally better performance on postlesion day 14 ($P = 0.0666$). The same analysis for the OLS group revealed significantly worse performance in the ON condition on postlesion day 3 ($P = 0.0471$) and marginally worse performance on postlesion day 5 ($P = 0.0554$) and postlesion day 8 ($P = 0.0781$) (Fig. S3). These effects tended to dissipate over time, so that no differences were detected between OFF and ON conditions in either group by postlesion day 21. These within-day differences through postlesion day 8 suggest that the timing of the S1 stimulus pulse is critical. Behavioral performance was significantly better when the S1 stimulus pulse was delivered contingent upon an action potential in the RFA (i.e., in the ADS group).

Effects of ADS on Functional Connectivity. To explore possible neurophysiological mechanisms underlying the behavioral effects of the ADS treatment on postinjury motor performance, we performed post hoc analysis of spike events in the RFA that were

discriminated in the 28 ms after each S1 stimulus pulse. This time window represented our imposed blanking period during which additional S1 stimulus pulses could not occur. Poststimulus spike histograms were compared with 28-ms periods chosen from data acquired in the OFF condition 7.5 ms after each RFA spike event. The results show that substantially more spikes in the RFA occurred following S1 stimulation in the ADS group, with peak activity occurring ~4–6 ms after the S1 stimulus pulse (Fig. 4A). Spike rates were nearly threefold higher averaged across the 28-ms period compared with a comparable period in the OFF condition. Spike rates in the OLS group were slightly lower than in the ADS group in the OFF condition but were significantly lower than in the ADS group in the ON condition. These data suggest that ADS substantially reinforced network interactions between S1 and the RFA, whereas OLS did not.

Subdividing the spike histograms by day reveals that enhanced spike activity in the ADS ON condition is evident even on the first day that the microdevice was activated (Fig. 4B and Fig. S4). There is also a trend toward further increases in spike discharge between the first (days 1 and 5) and second (days 8 and 14) weeks in the ADS group, corresponding to the time period when behavioral performance approached normal levels.

Whether behavioral performance and enhanced functional connectivity persist following the end of treatment cannot be addressed fully based on the current results (*SI Discussion*). However, it is noteworthy that there was a significant decrease in mean performance in the ADS group between postinjury days 21 and 28 (Fig. S5). During this time period, microelectrode-microdevice connection failures prevented normal operation of the microdevice in most of the ADS rats. This phenomenon of reduced behavioral performance after deactivation provides further
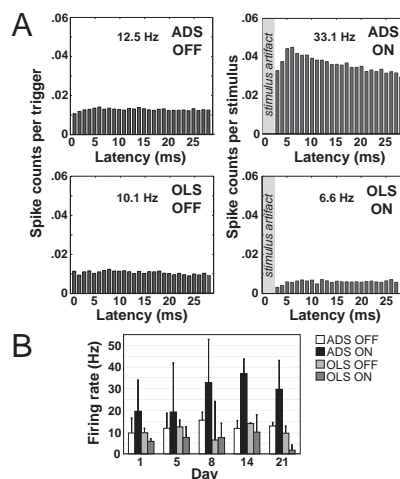

Fig. 4. Comparison of spike activity in the RFA in the ADS and OLS groups. Data represent spikes discriminated in the RFA over a 28-ms period. In the ON condition, the trigger for the data acquisition was the S1 stimulus pulse. In the OFF condition, the trigger for the data acquisition was 7.5 ms after a spike event in the RFA. (*A*) Composite posttrigger spiking histograms derived from neural recordings in the RFA compiled from days 1, 5, 8, 14, and 21 (±1 d). Histograms portray the mean spike counts per trigger event within each time bin (also Fig. S4). Spike counts were based on an average of over 22,000 trigger events per animal per day. Poststimulus firing rates were substantially higher in the ADS ON condition (33.1 Hz), compared with the ADS OFF (12.5 Hz), OLS ON (6.6 Hz), or OLS OFF (10.1 Hz) condition. (*B*) Average spike firing rates throughout the 28-ms window for each day. Error bars represent between-subject variation on each day (plus 1 SD). LMMs detected higher firing rates in the ADS group compared with the OLS group with stimulation ON ($P < 0.0001$). Firing rates did not differ statistically between groups in the OFF condition ($P > 0.05$). Posttrigger spiking histograms for each day are shown in Fig. S4.

support for the notion that the behavioral improvements were mediated by closed-loop operation. It also suggests that either a longer duration of operation (i.e., beyond 21 d) is required for persistent effects or that closed-loop stimulation enhances the rate, but not the extent, of recovery compared with OLS. Nonetheless, the present data provide persuasive evidence that targeted closed-loop stimulation approaches are feasible as brain repair strategies. Rapid behavioral recovery parallels the development of increased functional connectivity between spared somatosensory and motor regions of the cortex.

Discussion

This proof-of-concept study indicates that a closed-loop neuroprosthetic microdevice can enhance functional connectivity between distant cortical locations and generate rapid improvement in motor function after cortical injury, at least in rats with M1 damage. A closed-loop device with similar functionality induced neurophysiological changes when applied over a short distance within M1 of intact monkeys (15). More recently, spike-triggered stimulation was used to demonstrate increased potentiation between neurons in the sensorimotor cortex of rats. The spike-stimulation delay was important, because 5 ms resulted in robust increases, whereas 100 or 500 ms resulted in no potentiation (16). The present study demonstrates that the extension of the ADS approach to injured brains has demonstrable effects on recovery and establishes functional communication that is qualitatively different compared with uncorrelated stimulation. The current implementation of the system architecture, using a lightweight, battery-powered, wireless, miniaturized microdevice for spike-triggered intracortical microstimulation (ICMS), represents an important step in the process of developing implantable BMBIs for neural repair in clinical populations.

Differential Mechanisms Underlying the Effects of OLS and ADS on Behavioral Recovery. The mechanisms underlying the therapeutic effects of OLS and ADS after injury in the present model of TBI are still somewhat speculative. In the 1940s, Donald Hebb (17) postulated that "When one cell repeatedly assists in firing another, the axon of the first cell develops synaptic knobs... in contact with the soma of the second cell." This hypothesis has morphed into the modern maxim "Cells that fire together, wire together," a phrase made popular by neuroscientist, Carla Shatz (18). A large literature has grown from these initial hypotheses, and a neurophysiological phenomenon widely known as "Hebbian plasticity" has formed the basis for many neuroscientific models of learning and memory. Previous studies in intact primates and rodents using ADS or paired-pulse stimulation show the ability for such coactivation to alter output properties of cortical neurons (15, 16, 19). Presumably, the stimulation causes Hebbian-like plasticity to alter existing connectivity within a cortical area.

Although significant behavioral recovery occurred in both the ADS and OLS groups compared with control rats, the ADS group improved substantially more rapidly. Also, in the early postlesion period, the ADS group demonstrated a qualitatively different ON vs. OFF performance compared with the OLS group. These behavioral results alone suggest that different mechanisms underlie recovery in ADS and OLS groups. Although the results of ICMS on behavioral outcomes in animal models of brain injury have not been reported previously, several studies have examined the therapeutic effects of surface stimulation in either human stroke survivors or animal stroke models. For example, an invasive technology using epidural stimulation to provide low-level current pulses over uninjured cortical areas during the execution of rehabilitative training resulted in behavioral improvement in rodent and nonhuman primate models of cortical ischemic injury (20, 21). Although initial results in clinical stroke populations were promising, the therapeutic effect of open-loop epidural stimulation was not demonstrated in a randomized clinical trial (22). Nonetheless,

noninvasive cortical stimulation approaches (transcranial magnetic stimulation and transcranial direct-current stimulation) continue to attract substantial interest due to positive results in small groups of stroke survivors (23).

Evidence to support specific mechanisms underlying the effects of open-loop electrical stimulation of the cortex on recovery is largely correlative but includes motor map reorganization, increased dendritic length and spine density, cell proliferation and cell migration in the subventricular zone, receptor subunit expression, activation of antiapoptotic cascades, increased neurotrophic factors, enhanced angiogenesis, and proliferation of inflammatory cells (20, 21, 24–28). Because the number of stimulus pulses was similar in the ADS and OLS groups in the present study, it is reasonable to conclude that if electrical stimulation promoted proliferative processes, the effects were the same in the two groups.

In addition, various OLS protocols produce alterations in synaptic efficacy. These data are particularly relevant because of the qualitative differences in functional connectivity observed between ADS and OLS groups. Long-term potentiation (LTP), an experimental phenomenon first discovered in the hippocampus of anesthetized rabbits over 40 y ago (29), is expressed in both excitatory and inhibitory synapses throughout the mammalian brain (30). Although many experimental protocols have been developed to optimize synaptic potentiation in various model systems, the sign and magnitude of synaptic potentiation are heavily dependent upon the frequency and pattern of stimulation (31, 32).

Despite comparable mean stimulation frequency between the two groups, the temporal structure of stimulus pulses differed between the ADS and OLS groups. Interstimulus intervals spanned approximately the same range, but the intrinsic temporal firing pattern observed in the ADS group resulted in a greater number of short interstimulus intervals (Fig. S6A). Thus, ADS stimulation occasionally consisted of stimulus pulses at higher frequency, somewhat analogous to theta-burst stimulation, in which train bursts of high-frequency pulses (e.g., four to eight pulses at 100–300 Hz) are delivered at about 6–7 Hz (i.e., within the theta-rhythm frequency). Theta-burst stimulation is often used to optimize generation of LTP, especially in the neocortex of awake animals, where LTP has traditionally been more difficult to generate (33). In a study in the neocortex of freely moving rats, theta-burst stimulation, using parameters similar to those used in the hippocampus, evoked LTP, but the effects required at least 5 d to develop and plateaued at about 15 d (34). In the present study, although enhanced, short-latency spike discharge was evident with ADS even on the first day of stimulation, the time course of the behavioral effects was remarkably similar to the slowly developing LTP found in the rat neocortex study.

Theta-burst timing protocols vary considerably depending upon the particular model system. However, a recent study in a mouse brain slice preparation in the dorsal striatum suggests that the optimal theta-burst patterns are those that best match intrinsic neural activity patterns (35). Further, "burstiness" was critical to inducing LTP. Simply reducing the interburst pause from 35 ms to 20 ms eliminated the induction of LTP. It is possible that our imposed 28-ms blanking period further contributed to the neurophysiological and behavioral effects. We propose that by using a closed-loop stimulation paradigm, the intrinsic stimulation patterns that optimally drive synaptic potentiation in the cortico-cortical pathways were used. (The feasibility of using optimal theta-burst parameters in an open-loop mode of stimulation is discussed in *SI Discussion*).

In summary, OLS and ADS may both contribute to behavioral recovery but by somewhat different mechanisms. Electrical stimulation, in general, is likely to modulate neuronal growth processes, leading to adaptive plasticity that could account for at least part of the behavioral improvement. In the closed-loop (ADS) condition, however, the intrinsic firing pattern drives synaptic

potentiation in a manner similar to that observed in theta-burst protocols. Although potentiation builds rapidly (within 1 d), we propose that chronic ADS results in a behaviorally relevant, functional connection between S1 and PM.

Future Applications of Closed-Loop Neuroprostheses for Treating Neurological Disorders. A closed-loop neuroprosthesis applying ADS across distant cortical areas is a vastly different approach to brain repair than has been achieved to date. Therapeutic closed-loop stimulation in the brain is still uncommon. However, analogous approaches are already being tested for epilepsy, and an expanded role for closed-loop systems for deep brain stimulation in Parkinson disease is now being considered (36, 37). Further, closed-loop approaches are under development in animal models of spinal cord injury (38, 39). Other investigators have proposed a closed-loop approach for a cognitive prosthesis that has shown promise in animal models (40). Other potential clinical applications based on the current model include stroke, focal TBI, and surgical resections. Finally, a variety of neurological syndromes that are thought to be related to disruption of cortical communication may be amenable to ADS. In the 1960s, Norman Geschwind identified several disorders collectively called "disconnection syndromes," revolutionizing the field of behavioral neurology (41). The consideration of closed-loop approaches to repair of cortical disconnection syndromes may open treatment options for a variety of conditions in which neural communication is disrupted, whether due to disease, injury, or idiopathic causes.

Materials and Methods

Animals. Adult, male Long–Evans hooded rats ($n = 16$, weight: 350–450 g; Harlan) were procured at 4 mo of age. Protocols for animal use were approved by the Kansas University Medical Center Institutional Animal Care and Use Committee and adhered to the *Guide for the Care and Use of Laboratory Animals* (42). Each rat was singly housed in a transparent cage and provided with food and water ad libitum. The room was kept on a 12-h:12-h light/dark cycle, and ambient temperature was maintained at 22 °C.

Rats were assigned to three groups: the ADS group, the OLS group, and the control group. Rats in all three groups received a CCI injury over the M1 forelimb area (5). Postmortem histological analysis confirmed that lesion size was comparable across groups (*SI Results*). The surgical procedures (e.g., burr holes, skull screws, dura resection) were identical in all three groups. Microelectrode implantation and microdevice attachment were identical in the ADS and OLS groups. In both the ADS and OLS groups, one single-shank microelectrode array was inserted into the S1 forelimb area. A second single-shank microelectrode array was inserted into the RFA (depths are provided in *SI Materials and Methods*). In the ADS group, stimulation in S1 was contingent upon spike activity in the RFA; that is, time-amplitude window discriminators determined when action potentials were recorded from the RFA microelectrode. Discrimination of an individual action potential triggered delivery of a brief pulse of electrical current to the microelectrode implanted in S1. In the OLS group, the stimulation was delivered arbitrarily at a frequency approximately the same as that in the ADS group but with the timing of stimulation uncorrelated with the discriminated action potentials (*SI Materials and Methods*). The wireless, battery-powered microdevice, mounted to the freely moving rat's skull, operated 24 h per day (Fig. 2*A* and Fig. S1).

CCI Procedure. In each rat, the skull over the CFA was removed while leaving the dura intact. A 3-mm diameter rod with a flat tip was placed into a commercial impactor device (Leica Microsystems), centered over the target location (*SI Materials and Methods*), and then lowered until the surface of the tip was in contact with the dura, as indicated by an audible signal triggered by a feedback sensor. The rod was then retracted and armed. An impact was delivered with an excursion of 2 mm below the surface of the dura. This protocol leads to reproducible lesions that damage all cortical layers within the CFA with minimal superficial damage to underlying white matter tracts and limited or no damage to adjacent cortical areas (5).

Microdevice Programming. *ADS programming.* To determine discrimination parameters for ADS, the channel with the best signal-to-noise ratio was chosen. This same channel was later used during microdevice operation to determine spike events that triggered stimulation. Using a custom MATLAB

(MathWorks) script, action potentials were discriminated offline by thresholding and two user-adjustable time-amplitude windows, with the intent of maximizing discrimination of observed spikes while minimizing noise and/or stimulus artifacts. Stimulation parameters were set to deliver a 60-μA, 192-μs, pseudobiphasic current pulse with a 7.5-ms delay following spike discrimination (Fig. 2*B*). A blanking interval following each spike discrimination prevented additional stimulus pulses for 28 ms. The spike discrimination, timing, and stimulation parameters were then uploaded to the microdevice for online spike discrimination. Thus, during device operation in the ADS group, each discriminated spike in PM triggered a stimulation pulse in S1, constrained by the blanking interval.

The 7.5-ms delay was based on previous studies of the effective delay within local networks, analysis of spike-stimulus delays in pilot data, as well as constraints in the current microdevice architecture. The 28-ms blanking interval was also based on analysis of spike-stimulus delays in pilot data and was set to reduce the possibility of producing a positive-feedback loop, in which S1 stimulation might drive action potentials in PM, retriggering stimulation of S1.
OLS programming. Stimulation parameters were the same in the OLS group as for the ADS group. However, the stimulation was not contingent upon recorded neural activity. Instead, the stimulation was set to occur arbitrarily with interstimulus intervals ranging from 35 to 200 ms (randomized equally across the range), closely approximating the stimulus rate for the ADS group (*SI Materials and Methods*, *SI Results*, and Fig. S6*A*).
Signal monitoring and maintenance. The neural activity and stimulation rates were monitored daily throughout the study via a wireless connection. The microdevice ran continuously, delivering ADS or OLS 24 h a day during the experiment, except for brief periods required for behavioral assessment, changing the battery, and adjusting the window discriminator parameters.

Bandpass-filtered neural data (~500 Hz to 5 kHz) were recorded at ~35.7 kHz per channel from either one or four channels (wireless or wired connection, respectively) during all signal monitoring and behavioral trials using LabVIEW software (National Instruments). In addition, all animals had multiple sessions during which data were recorded during home cage behavior. The raw signal recording duration of any single monitoring period was software-limited to ~45 min, but the stimulus trigger signal could be recorded for up to 24 h. The neural signal data were converted from a LabVIEW file to a text file and analyzed using custom MATLAB software.

Behavioral Training and Assessment. *Skilled reaching task.* Each rat was tested in a 30-cm × 30-cm × 52-cm Plexiglas reaching chamber. For each trial, a single food pellet (45 mg; Bioserv) was placed into a shallow well 2 cm from the front wall on an external shelf positioned 3 cm from the bottom of the chamber. The rat was required to reach through a narrow slot to retrieve the pellet with its forepaw (Fig. 2*A*). After forelimb preference was determined, a removable Plexiglas wall was used to force the animal to use only the preferred forelimb (5). Trials were recorded with a digital camcorder for playback and analysis. The percentage of success was measured as the percentage of trials in which the rat grasped, retrieved, and brought the pellet to the mouth (60 trials per day). Before entry into the remainder of the study, the rat was required to reach and retrieve food pellets above 70% success for 3 consecutive days. Following the injury (see below), behavioral probing sessions were conducted on postlesion days 3, 5, 8, 14, 21, and 28. Testing on postlesion days 1 and 2 was not practical due to the effects of surgical recovery and postsurgical analgesics on behavioral performance. Probing sessions consisted of 20 trials with the microdevice stimulation function turned OFF and then 20 trials with the microdevice stimulation function turned ON.
Foot-fault task. Rats were also assessed on a foot-fault task to determine the effects of the injury on a locomotion task. In general, although there was an effect of the injury on this task on postlesion day 3, no lesion effects were observed on subsequent days. Also, there were no differences between groups at any time points. This result was not unexpected, because the foot-fault task is less sensitive, and spontaneous recovery is common with lesions restricted to the forelimb motor cortex.

Statistical Analysis of Behavioral Performance. Initially, animals were randomly assigned to an ADS ($n = 6$) or control ($n = 5$) group. A subsequent OLS group ($n = 5$) was studied after group randomization. This was necessary to use neurophysiological data from the ADS group to determine the stimulation protocol for the OLS group.

Linear mixed models (LMMs) (43) were generated via restricted maximum likelihood estimation using SAS version 9.2 PROC GLIMMIX (SAS Institute, Inc.) to model performance on the skilled reaching task for each animal over time. Results are presented to mirror a series of one-way ANOVA models because the LMM provides analogous results. For animals in the ADS and

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OLS groups, the difference between the OFF and ON conditions was studied as an outcome. Models included fixed effects for treatment group, time, and their interaction.

Time was treated as a continuous measure to generate estimates of a polynomial relationship for recovery profiles in each treatment group over time up to a (treatment group-specific) quadratic relationship. Animal-specific effects were introduced by allowing for random intercepts in these models; thus, the models allowed for estimation of normally distributed error terms both for between- and within-animal effects. Backward elimination was used to determine the functional form of these relationships with F test P values <0.05 for effects to remain in the models. All lower ordered terms were retained in models in the presence of higher level interaction effects, regardless of statistical significance. Models were evaluated by visual inspection of observed vs. predicted values for each animal to assess model fit, observed vs. residuals plots to assess constant variance assumptions, and histograms of the residuals and quantile-quantile plots to assess the assumption of normally distributed random effects. Residuals included both those for the random intercept coefficients (for between-animal error terms) and overall residuals (for within-animal error terms).

Linear contrasts of model estimates were used to test for treatment group differences on postlesion days 3, 5, 8, 14, 21, and 28 using F tests, with day 28 serving as the a priori time point of interest for the comparison of ADS vs. OLS. Other pairwise comparisons at each time point were also tested (*SI Materials and Methods*, *Protocol Deviations*). Given the single, a priori primary comparison, no further adjustments for multiple comparisons were made. Linear contrasts were used to generate 95% confidence intervals for each treatment group for those specific days and, within the ADS and OLS groups, to test for differences in the OFF vs. ON conditions. Two-sided P values were used for presentation of results.

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